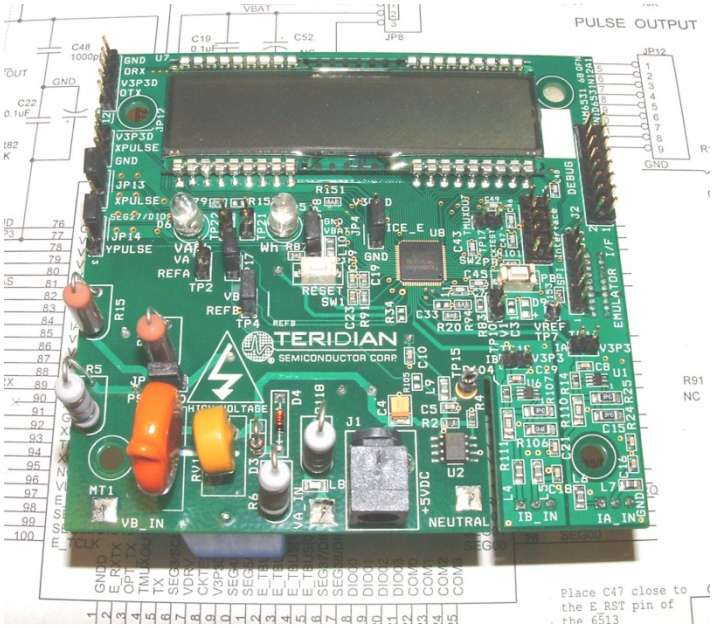
71M6531 Demo Board

USER'S MANUAL



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71M6531

Single-Phase Energy Meter IC

DEMO BOARD

USER'S MANUAL

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1 GETTING STARTED

1.1 GENERAL

The TERIDIAN Semiconductor Corporation (TSC) 71M6531 Demo Board is an energy meter IC demonstration board for evaluating the 71M6531D/F device for residential electronic energy metering applications. It incorporates a 71M6531D/F integrated circuit, peripheral circuitry such as a serial EEPROM, emulator port, and on-board power supply as well as a companion Debug Board that allows a connection to a PC through a RS232 port. The Demo Board allows the evaluation of the 71M6531D/F energy meter controller chip for measurement accuracy and overall system use.

The board is pre-programmed with a Demo Program (file name 6531_demo.hex) in the FLASH memory of the 71M6531D/F IC. This embedded application is developed to exercise all low-level functions to directly manage the peripherals and CPU (clock, timing, power savings, etc.).

1.2 SAFETY AND ESD NOTES

Connecting live voltages to the Demo Board system will result in potentially hazardous voltages on the Demo Board.

EXTREME CAUTION SHOULD BE TAKEN WHEN HANDLING THE DEMO BOARD ONCE IT IS CONNECTED TO LIVE VOLTAGES!

THE DEMO SYSTEM IS ESD SENSITIVE! ESD PRECAUTIONS SHOULD BE TAKEN WHEN HANDLING THE DEMO BOARD!

1.3 DEMO KIT CONTENTS

- 71M6531 Demo Board containing 71M6531D/F IC with preloaded Demo Program and prepared for either CT or shunt resistor operation
- Debug Board
- Shunt resistor with wire harness, 400µΩ (for kits shipped in shunt configuration)
- Two 5VDC/1,000mA universal wall transformers w/ 2.5mm plug (Switchcraft 712A)
- Serial cable, DB9, Male/Female, 2m length (Digi-Key AE1379-ND)
- CD-ROM containing documentation (data sheet, board schematics, BOM, layout), Demo Code, and utilities

Note: The CD-ROM contains a file named **readme.txt** that specifies all files found on the media and their purpose.

1.4 COMPATIBILITY

This manual applies to the following hardware and software revisions:

- 71M6531D/F, chip revision A03
- Demo Boards D6531N12A2
- Demo Board Code revision 6531_4p6q_12may08_0cc.hex, 6531_4p6q_12may08_0sc.hex (EQU 0) , 6531_4p6q_12may08_1cc.hex EQU 1), 6531_4p6q_12may08_2cc.hex (EQU 2), or later

1.5 SUGGESTED EQUIPMENT NOT INCLUDED

For functional demonstration:

- PC w/ MS-Windows® versions XP, ME, or 2000, equipped with RS232 port (COM port) via DB9 connector
- One or two current transformers (CTs), preferably 2,000:1 turns ratio
- For software development (MPU code):
- Signum ICE (In Circuit Emulator): ADM-51
- http://www.signum.com
- Keil 8051 "C" Compiler kit: CA51

http://www.keil.com/c51/ca51kit.htm, http://www.keil.com/product/sales.htm

1.6 DEMO BOARD TEST SETUP

Figure 1-1 shows the basic connections of the Demo Boards plus Debug Boards with the external equipment.

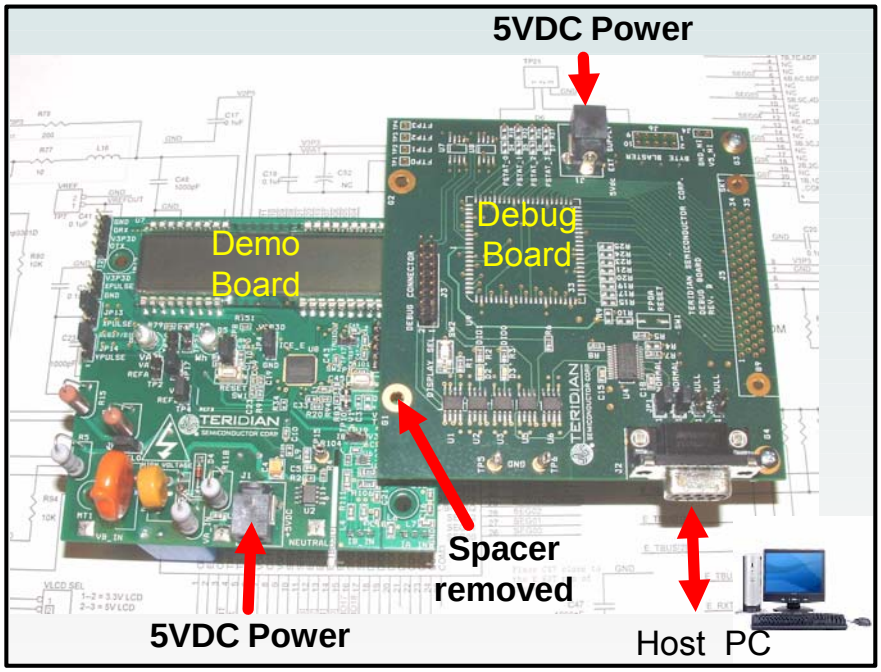


Figure 1-1: Demo Board: Basic Connections

The Debug Board can be plugged into J2 of the Demo Board. One spacer of the Debug Board should be removed, as shown in Figure 1-1. Alternatively, both boards can be connected using a flat ribbon cable, as shown in Figure 1-2. A male header has to be soldered to J3 of the Debug Board, and the female-to-female flat ribbon cable is not supplied with the Demo Kit (use Digi-Key P/N A3AKA-1606M-ND or similar).

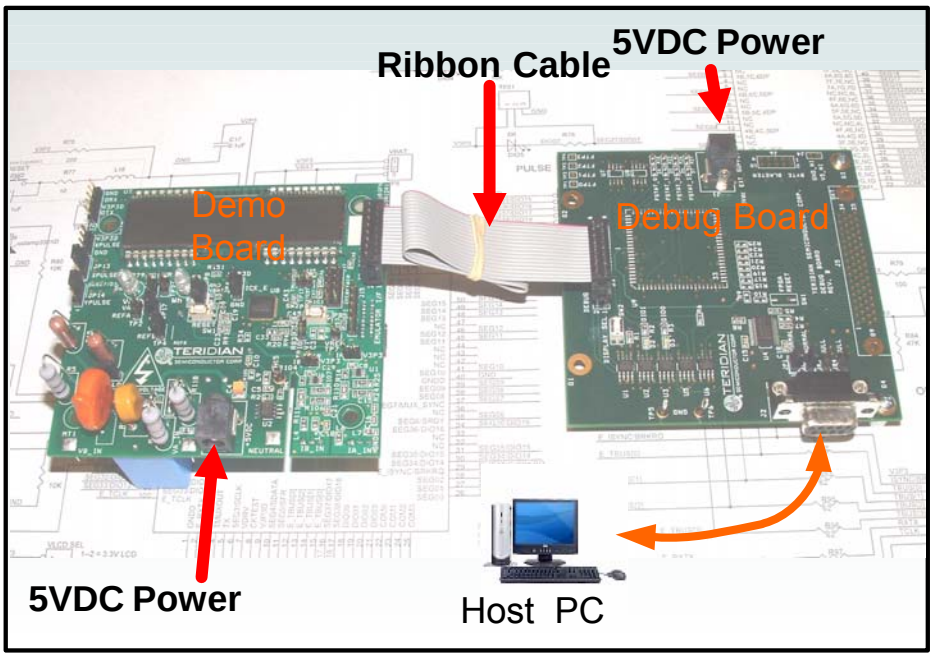


Figure 1-2: Demo Board: Ribbon Cable Connections

The 71M6531 Demo Board block diagram is shown in Figure 1-3. It consists of a stand-alone meter Demo Board and an optional Debug Board. The Demo Board contains all circuits necessary for operation as a meter, including display, calibration LED, and power supply. The Debug Board, when not sharing a power supply with the meter, is optically isolated from the meter and interfaces to a PC through a 9 pin serial port.

Connections to the external signals to be measured, i.e. scaled AC voltages and current signals derived from shunt resistors or current transformers, are provided on the rear side of the Demo Board.

It is recommended to set up the Demo Board with no live AC voltage connected, and to connect live AC voltages only after the user is familiar with the demo system.

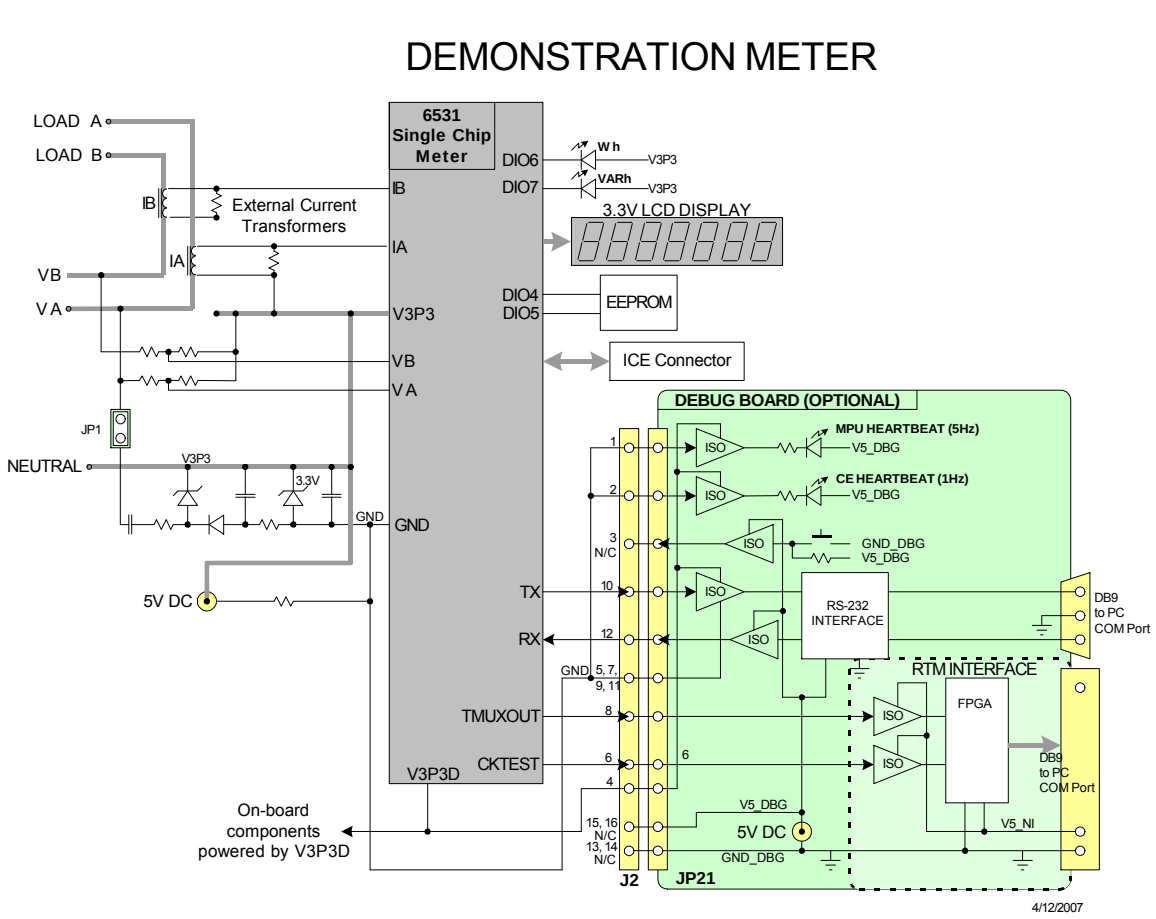


Figure 1-3: The TERIDIAN 6531 Demo Board with Debug Board Block Diagram (CT Configuration)

Note: All analog input signals are referenced to the V3P3A net (3.3V power supply to the chip).

1.6.1 POWER SUPPLY SETUP

There are several choices for meter the power supply:

- Internal (using the AC line voltage). The internal power supply is only suitable when the line voltage exceeds 220V RMS.
- External 5VDC connector (J1) on the Demo Board
- External 5VDC connector (J1) on the Debug Board.

The power supply jumper, JP1, must be consistent with the power supply choice. JP1 connects the AC line voltage to the internal power supply. This jumper should usually be left in place.

When the Demo Board is in shunt configuration, the shunt resistor has to be connected as shown in Figure 1-7 for the board to be powered via J1. Alternatively, a jumper cable between any header labeled V3P3 and the NEUTRAL terminal (J9) can be supplied.

1.6.2 CABLE FOR SERIAL CONNECTION

For connection of the DB9 serial port to a PC, either a straight or a so-called "null-modem" cable may be used. JP1 and JP2 are plugged in for the straight cable, and JP3/JP4 are empty. The jumper configuration is reversed for the null-modem cable, as shown in Table 1-3.

Cable Configuration	Mode	Jumpers on Debug Board			
		JP1	JP2	JP3	JP4
Straight Cable	**Default**	Installed	Installed	--	--
Null-Modem Cable	Alternative	--	--	Installed	Installed

Table 1-1: Jumper settings on Debug Board

JP1 through JP4 can also be used to alter the connection when the PC is not configured as a DCE device. Table 1-2 shows the connections necessary for the straight DB9 cable and the pin definitions.

PC Pin	Function	Demo Board Pin
2	TX	2
3	RX	3
5	Signal Ground	5

Table 1-2: Straight cable connections

Table 1-3 shows the connections necessary for the null-modem DB9 cable and the pin definitions.

PC Pin	Function	Demo Board Pin
2	TX	3
3	RX	2
5	Signal Ground	5

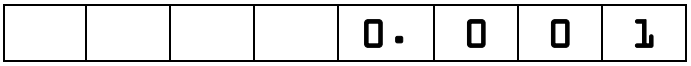
Table 1-3: Null-modem cable connections

1.6.3 CHECKING OPERATION

A few seconds after power up, the LCD display on the Demo Board should briefly display the following welcome text:

After the "HELLO" text, the LCD should display the following information:

and:



The text "Wh" indicates that accumulated Watt-hours are displayed. In the case shown above, 0.001 Wh were accumulated. The display will be cycling from numeric to text, indicating activity of the MPU inside the 71M6531D/F.

In Mission Mode, the display can be cycled to display VARh, PF and other parameters by pressing the pushbutton (PB).

1.6.4 SERIAL CONNECTION SETUP FOR THE PC

After connecting the DB9 serial port to a PC, start the HyperTerminal application (or any other suitable communication program) and create a session using the communication parameters shown in Table 1-4.

Setup Parameter	Value
Port speed (baud)	9600/300†
Data bits	8
Parity	none
Stop bits	1
Flow control	XON/XOFF
	† depending on the jumper setting at JP12

Table 1-4: COM Port Setup Parameters

HyperTerminal can be found by selecting Programs →Accessories → Communications from the Windows© start menu. The connection parameters are configured by selecting File → Properties and then by pressing the Configure button (see Figure 1-4).

A setup file (file name "Demo Board Connection.ht") for HyperTerminal that can be loaded with File → Open is also provided with the tools and utilities on the supplied CD-ROM.

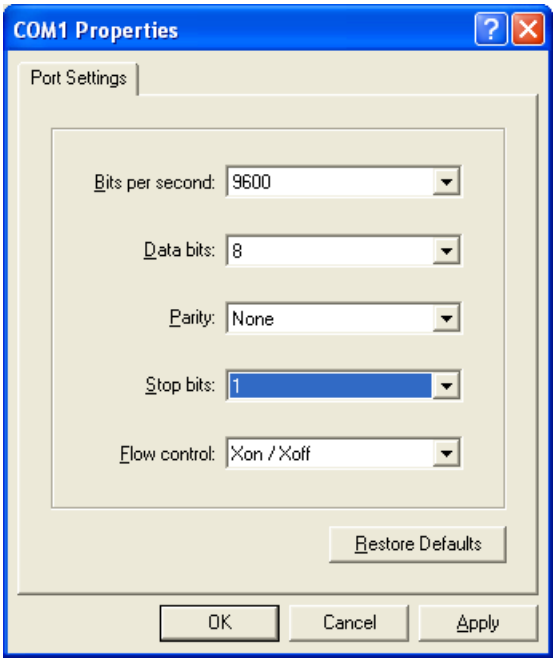


Figure 1-4: Port Configuration Setup

Note: Port parameters can only be adjusted when the connection is not active. The disconnect button, as shown in Figure 1-5 must be clicked in order to disconnect the port.

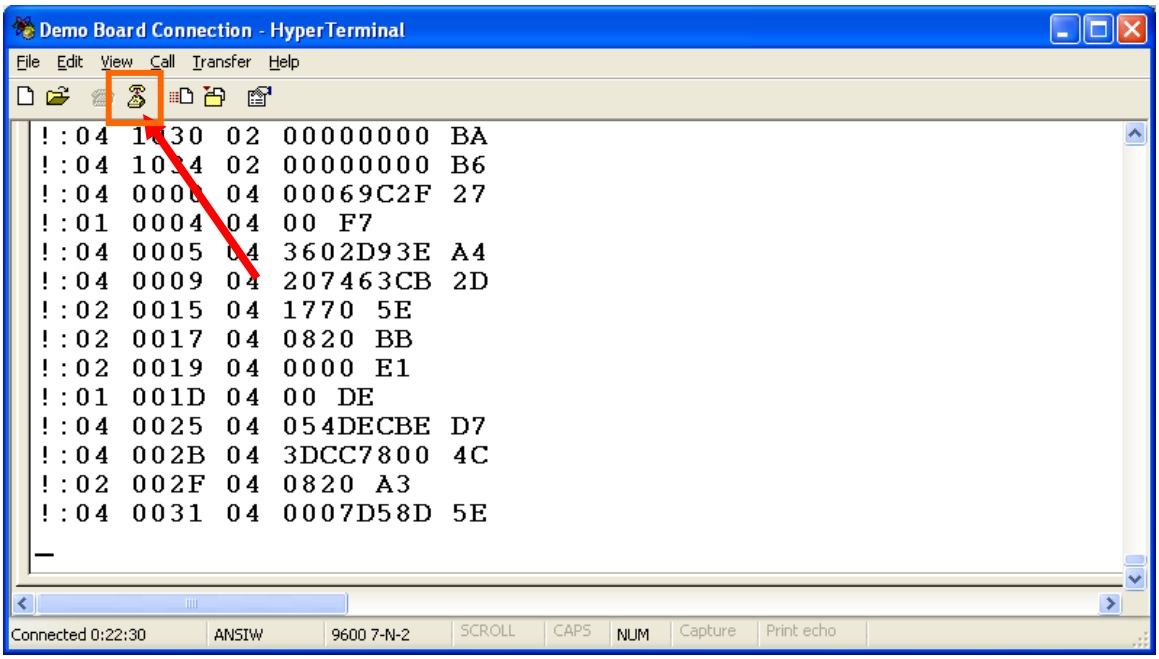


Figure 1-5: Hyperterminal Sample Window with Disconnect Button

1.7 USING THE DEMO BOARD

The 71M6531 Demo Board is a ready-to-use meter prepared for use with an external shunt resistor.

Using the Demo Board involves communicating with the Demo Code. An interactive command line interface (CLI) is available as part of the Demo Code. The CLI allows modifications to the metering parameters, access to the EEPROM, initiation of auto-calibration sequences, selection of the displayed parameters, changing calibration factors and many more operations.

Before evaluating the 71M6531 Demo Board, users should get familiar with the commands and responses of the CLI. A complete description of the CLI is provided in section 1.7.2.

1.7.1 CYCLING THE LCD DISPLAY

The Demo Codes for the 71M6531 Demo Board allow cycling of the display using the PB button. By briefly pressing the button, the next available parameter from Table 1-5 is selected. This makes it easy to navigate various displays for Demo Boards that do not have the CLI.

Step	Text Display	Displayed Parameter
1	Wh	Accumulated real energy [Wh]. The default display setting after power-up or reset.
2	VARh	Accumulated reactive energy [VARh].
3	Hours	Expired hours after power-up or reset
4	Time	Time of day (hh.mm.ss).
5	Date	Date (yyyy.mm.dd).
6	PF	Current power factor.
7	Edges	Count of zero crossings in the last accumulation interval.
8	Pulses	Number of emitted pulses.
8	A	RMS current at phase A input [A].
8	V	RMS voltage at the VA_IN input [V].
8	Bat V	Measured battery voltage [V].
8	Delta T	Temperature difference from calibration temperature. Displayed in 0.1°C

Table 1-5: Selectable Display Options

1.7.2 SERIAL COMMAND LINE INTERFACE (CLI)

Once, communication to the Demo Board is established, press <CR> and the Demo Program prompt ("**>**") should appear. Type **>i** to verify that the Demo Program version is revision 4p6q or later.

Users should familiarize themselves with the Demo Program commands described in the tables below.

The Demo Program (Demo Code) is compiled with EEPROM specified as the non-volatile memory. This means that the default calibration factors are stored in flash memory while the calibration factors resulting from an actual calibration are stored in EEPROM.

The tables below describe the commands in detail. Type '?' for a display of available commands.

Commands for CE Data Access:

]	CE DATA ACCESS	Remarks
Description:	Allows user to read from and write to CE data space.	
Usage:	] [Starting CE Data Address] [option]…[option]	
Command combinations:	]???	Read consecutive 16-bit words in Decimal
	]$$$	Read consecutive 16-bit words in Hex
	]U	Update default version of CE Data in EEPROM. **Important: The CE must be stopped (CE0) before issuing this command!**
Example:	]40$$$	Reads CE data words 0x40, 0x41 and 0x42.
	]7E=12345678=9876ABCD	Writes two words starting @ 0x7E

CE data space is the address range from 0x1000 to 0x13FF. All CE data words are in 4-byte (32-bit) format. The offset of 0x1000 does not have to be entered when using the] command, thus typing]A? will access the 32-bit word located at the byte address 0x1000 + 4 * A = 0x1028.

Commands for MPU/XDATA Access:

)	MPU DATA ACCESS	Remarks
Description:	Allows user to read from and write to MPU data space.	
Usage:	) [Starting MPU Data Address] [option]…[option]	
Command combinations:	)???	Read three consecutive 32-bit words in Decimal
	)$$$	Read three consecutive 32-bit words in Hex
	)a=n=m	Write the values n and m to two consecutive addresses starting at a
Example:	)08$$$$	Reads data words 0x08, 0x0C, 0x10, 0x14
	)04=12345678=9876ABCD	Writes two words starting @ 0x04

MPU or XDATA space is the address range for the MPU XRAM (0x0000 to 0x0FFF). All MPU data words are in 4-byte (32-bit) format. Typing]A? will access the 32-bit word located at the byte address 4 * A = 0x28. The energy accumulation registers of the Demo Code can be accessed by typing two question marks ("??").

Commands for I/O RAM (Configuration RAM) and SFR Control:

R	DIO AND SFR CONTROL	Remarks
Description:	Allows the user to read from and write to I/O RAM and special function registers (SFRs).	
Usage:	R [option] [register] … [option]	
Command combinations:	RIx…	Select I/O RAM location x (0x2000 offset is automatically added)
	Rx…	Select internal SFR at address x
	Rx???...	Read consecutive SFR registers in decimal
	Rx$$$...	Read consecutive registers in hex notation
Example:	RI60$$$$	Read all four RTM probe registers

DIO or Configuration RAM space is the address range 0x2000 to 0x20FF. This RAM contains registers used for configuring basic hardware and functional properties of the 71M6531D/F and is organized in bytes (8 bits). The 0x2000 offset is automatically added when the command RI is typed. The SFRs (special function registers) are located in internal RAM of the 80515 core, starting at address 0x80.

Commands for EEPROM Control:

EE	EEPROM CONTROL	Remarks
Description:	Allows user to enable read and write to EEPROM.	
Usage:	EE [option] [arguments]	
Command combinations:	EECn	EEPROM Access (1 → Enable, 0 → Disable)
	EERa.b	Read EEPROM at address 'a' for 'b' bytes.
	EEE	Erase the EEPROM
	EESabc..xyz	Write characters to buffer (sets Write length)
	EETa	Transmit buffer to EEPROM at address 'a'.
	EEWa.b...z	Write values to buffer
Example:	EEShello; EET$0210	Writes 'hello' starting at EEPROM address 0x210.

The EEC1 command must be issued before the EEPROM interface can be used. The execution of the EEE command takes several seconds. During this time, no other commands can be entered.

Auxiliary Commands:

	AUXILIARY	Remarks
Description:	Various	
Commands:	,	Typing a comma (",") repeats the command issued from the previous command line. This is very helpful when examining the value at a certain address over time, such as the XRAM address for the temperature.
	/	The slash ("/") is useful to separate comments from commands when sending macro text files via the serial interface. All characters in a line after the slash are ignored.
	?	Displays the help menu.
	CLC	Enables communication via hex records.
	BT	Commands execution of a battery test.

Commands controlling the CE:

C	COMPUTE ENGINE CONTROL	Remarks
Description:	Allows the user to enable and configure the compute engine.	
Usage:	C [option] [argument]	
Command combinations:	CEn	Compute Engine Enable (1 → Enable, 0 → Disable)
	CTn	Select input n for TMUX output pin. Enter n in hex notation.
	CREn	RTM output control (1 → Enable, 0 → Disable)
	CRSa.b.c.d	Selects CE addresses for RTM output (maximum of four)
Example:	CE0	Disables the CE
	CT1E	Selects the CE_BUSY signal for the TMUX output pin

Calibration Commands:

CL	CALIBRATION CONTROL	Remarks
Description:	Calibration-related commands. A full auto-calibration can be implemented by compiling the Demo Code with auto-calibration selected as an option. Due to space restrictions, the auto-calibration is not implemented in the Demo Code supplied with the Demo Boards.	
Usage:	CL [option]	
Command combinations:	CLC	Loads a calibration via serial port
	CLB	Starts an auto-calibration sequence
	CLD	Restores calibration to defaults
	CLR	Restores calibration from EEPROM
	CLS	Saves calibration to EEPROM

Commands for Identification and Information:

I	INFORMATION MESSAGES	Remarks
Description:	Allows user to display information messages.	
Usage:	I	
Example:	I	Returns the Demo Code version

The I command is used to identify the revisions of Demo Code and the contained CE code.

Commands for Controlling the Metering Values Shown on the LCD Display:

M	METER DISPLAY CONTROL (LCD)	Remarks
Description:	Allows user to select internal variables to be displayed.	
Usage:	M [option]. [option]	
Command combinations:	M	kWh Total Consumption (display wraps around at 999.999)
	M1	Temperature (C° delta from nominal)
	M2	Frequency (Hz)
	M3. [phase]	kWh Total Consumption (display wraps around at 999.999)
	M4. [phase]	kWh Total Inverse Consumption (display wraps around at 999.999)
	M5. [phase]	kVARh Total Consumption (display wraps around at 999.999)
	M6. [phase]	kVAh Total Inverse Consumption (display wraps around at 999.999)
	M7. [phase]	VAh Total (display wraps around at 999.999)
	M9	Real Time Clock
	M10	Calendar Date
	M13. n	Main edge count (n = 0: accumulated, n = 1: last second)
	M17	Battery voltage. Display will return to M3 after a few seconds.
Example:	M3.1	Displays Wh total consumption of phase A.

Displays for total consumption wrap around at 999.999kWh (or kVARh, kVAh) due to the number of available display digits. Internal registers (counters) of the Demo Code are 64 bits wide and do not wrap around.

The internal accumulators in the Demo Code use 64 bits and will neither overflow nor wrap around under normal circumstances. The restriction to only six digits is due to the requirement to provide one digit showing the display mode that is separated by a blank digit from the displayed values.

Commands for Controlling the RMS Values Shown on the LCD Display:

MR	METER RMS DISPLAY CONTROL (LCD)	Remarks
Description:	Allows user to select meter RMS display for voltage or current.	
Usage:	MR [option]. [option]	
Command combinations:	MR1. [phase]	Displays instantaneous RMS current
	MR2. [phase]	Displays instantaneous RMS voltage
Example:	MR1.2	Displays phase b RMS current.

Commands for Controlling the MPU Power Save Mode:

PS	POWER SAVE MODE	Remarks
Description:	Enters power save mode	Disables CE, ADC, CKOUT, ECK, RTM, TMUX VREF, and serial port, sets MPU clock to 38.4KHz.
Usage:	PS	

Return to normal mode is achieved by issuing a hardware reset.

Commands for Controlling the RTC:

RT	REAL TIME CLOCK CONTROL	Remarks
Description:	Allows the user to read and set the real time clock.	
Usage:	RT [option] [value] … [value]	
Command combinations:	RTDy.m.d.w: Day of week	(year, month, day, weekday [1 = Sunday]). Weekday is automatically set if omitted.
	RTR	Read Real Time Clock.
	RTTh.m.s	Time of day: (hr, min, sec).
	RTAs.t	Real Time Adjust: (speed, trim)
Example:	RTD05.03.17.5	Programs the RTC to Thursday, 3/17/2005

Reset Commands:

Z, W	RESET	Remarks
Description:	Allows the user to cause soft or watchdog resets	
Usage:	Z	Soft reset
	W	Simulates watchdog reset

The Z command acts like a hardware reset. The energy accumulators in XRAM will retain their values.

Commands for Controlling the LCD and Sleep Modes (when in Brownout Mode):

B	POWER MODE CONTROL	Remarks
Description:	Allows the user switch to LCD and Sleep mode when the 71M6531D/F is in Brownout mode.	
Usage:	B [option] [value]	
Command combinations:	BL	Enters LCD mode
	BS	Enters Sleep mode
	BWSn	Prepares Sleep mode with the wakeup timer set to n seconds
	BWMm	Prepares Sleep mode with the wakeup timer set to m minutes
Example:	BWS8 BS	Enters Sleep mode with the wakeup timer set to 8 seconds. The 71M6531D/F will enter Sleep mode and return to Brownout mode after 8 seconds.

Commands for Error Recording:

ER	ERROR RECORDING	Remarks
Description:	Allows the user display and clear the error log.	
Usage:	ER [option] [value]	
Command combinations:	ERC	Clears all errors from error log
	ERD	Displays error log
	ERS+n	Enters error number n in error log
Example:	ERS+10	Enters error number 10 in error log

1.7.3 COMMUNICATING VIA INTEL HEX RECORDS

Communication with the 71M6531D/F IC, especially by computers and/or ATE, may also be accomplished using a simplified protocol based on Intel Hex records. These records can still be sent and received with an ordinary terminal, and coding and decoding of commands and responses is straight-forward.

Using the Hex-Record Format

Intel's Hex-record format allows program or data files to be encoded in a printable (ASCII) format, allowing editing of the object file with standard tools and easy file transfer between a host and target. An individual hex-record is a single line in a file composed of one or several Hex-records.

Entering "CLC" from the text-based command line interface enables the hex-record interface.

Hex-Records are character strings made of several fields which specify the record type, record length, memory address, data, and checksum. Each byte of binary data is encoded as a 2-character hexadecimal number: the first ASCII character representing the high-order 4 bits, and the second the low-order 4 bits of the byte. The six fields that comprise a Hex-record are defined in Table 1-6.

Field	Name	Characters	Description
1	Start code	1	An ASCII colon (":")
2	Byte count	2	The count of the character pairs in the data field.
3	Address	4	The 2-byte address at which the data field is to be loaded into memory. This is the physical XRAM or I/O RAM address, not the 4-byte address used by the command-line interface (CLI).
4	Type	2	00, 01, or 02.
5	Data	0-2n	From 0 to n bytes of executable code, or memory loadable data. n is normally 20 hex (32 decimal) or less.
6	Checksum	2	The least significant byte of the two's complement sum of the values represented by all the pairs of characters in the record except the start code and checksum.

Table 1-6: Fields of a Hex Record

Each record may be terminated with a CR/LF/NULL character. Accuracy of transmission is ensured by the byte count and checksum fields. This is important when series of values such as calibration constants are transmitted to a meter, e.g. by ATE equipment in a factory setting. When entering hex records manually, the user may also choose "FF" ("wild card") as the checksum. In this case, the Demo Code omits comparing the checksum with the received record(s).

This is how the checksum is calculated manually (if necessary):

1) The hex values of all bytes (except start code and checksum itself) are added up.

2) The last two hex digits are subtracted from 0xFF.

3) The value 0x01 is added.

As opposed to the standardized Hex-records that offer three possible types (data, termination, segment base), six different types are supported for communicating with the 71M6531D/F. These data types basically encode command types (read/write) along with the data source or destination, as listed in Table 1-7.

Number	Code	Function
1	00	Write CE data record, contains data and 16-bit CE address (CE data RAM is located at 0x1000).
2	01	End Of File (Quit) record, a file termination record. Contains no data. This record has to be the last line of the file, and only one record per file is permitted. The byte pattern is always ':00000001FF'. Upon receipt of this record, the Demo Code will transfer the received data into non-volatile memory (EEPROM).
3	02	Alternate form of Write CE data record (optional). CE data RAM is located at 0x1000.
4	03	Read CE data record, contains empty data field and 16-bit CE address (optional). CE data RAM is located at 0x1000.
5	04	Write MPU or I/O RAM data record, contains data and 16-bit MPU address.
6	05	Read MPU or I/O RAM data record, contains empty data field and 16-bit MPU address (optional). I/O RAM is located at 0x2000.
7	06	Write RTC data record, contains data and 16-bit RTC address.
8	07	Read RTC data record, contains empty data field and 16-bit RTC address (optional).
9	08	Write SFR data record, contains data and 16-bit SFR address (optional). The MSB is always zero (0).
10	09	Read SFR data record, contains empty data field and 16-bit SFR address (optional).

Table 1-7: Data (command) types

Table 1-8 lists a few examples of hex records.

Hex Record	Function
`:08 0000 06 00 00 0C 03 18 05 06 00 ff`	Writes (06) eight bytes (08) to RTC, setting the RTC to zero seconds (00), minutes (00), 12 hours (0C), Wednesday (03), 24th (18) of May (05), 2006 (06). Uses the wild card checksum.
`:10 0010 00 00004000 00004000 00004000 00004000 E8` `:00 0000 01 FF`	Writes the default values (0x4000) for the calibration constants CAL_IA, CAL_IB, CAL_VA, and CAL_VC to the XRAM (00), starting at address 0x10 (0010). The second command causes the Demo Code to write the data to permanent storage.
`:10 1020 03 FF`	Causes the Demo Board to display the CE data from address 0x1020 to 0x102F

Table 1-8: Hex Record examples

The Demo Board will not echo any inputs from the terminal (they screen will stay blank except for the asterisk (*****) issued after the user enters <CR><LF>). It is useful to configure Hyperterminal for "auto-echo". This can be done by selecting "Properties" from the "File" menu, then clicking on the "Settings" tab and clicking the "ASCII Setup" button.

No <ENTER> key is necessary at the end of a manually entered record.

Spaces in between the fields (to increase readability), as in the example above, are ignored by the Demo Boards.

If a hex record is accepted, the Demo Board returns a "**!**". If the hex record is not accepted, the Demo Board sends a "**?**" and other text, depending on the context (only the 16KB Demo Code will send text). When only a partial record is entered, the Demo Board will time out after around 30 seconds and then send <CR>< LF>.

A number of pre-assembled hex records is supplied with the Demo Code. It is easier to send a pre-assembled record using the "send text file" feature in the "Transfer" menu of Hyperterminal, than assembling hex record from scratch.

The pre-assembled hex records are contained in a ZIP file named 6531_scripts.zip on the CD-ROM supplied with the Demo Kits. Table 1-9 shows the records available and their function.

Hex Record Name	Function
set_6531_defaults.txt	Sets the default configuration, including all CE variables. Transferring this record is necessary when data in the EEPROM is lost or compromised.
read_6531_temp.txt	Displays the current temperature reading from the CE
set_6531_temp.txt	This record can be edited to set the nominal (calibration) temperature
read_6531_power.txt	Displays the valid power data
read_6531_ce.txt	Displays CE data from memory locations 0x1020 to 0x10FF
read_6531_config.txt	Displays configuration data. This hex record includes comment text helping to interpret the received data.
set_6531_rtm.txt	Sets up the real-time monitor

Table 1-9: Pre-assembled hex records

1.7.4 USING THE BATTERY MODES

The 71M6531D/F is in so-called Mission mode, as long as 3.3VDC is supplied to the V3P3SYS pin. If this voltage is below the minimum required operating voltage which is usually indicated by V1 < 1.6 (internal VBIAS voltage), and if no battery is connected to the VBAT pin, the chip is powered off.

Battery modes can be used if a battery or other DC source supplying a DC voltage with in the operating limits for the battery input is applied to the battery pin (VBAT, pin 49) of the chip. On the Demo Board, the battery should be connected to pin 2 (+) and 3 (-) of JP8.

In order to prevent corruption of external memory, which could occur when main power is removed from the Demo Board while no battery is present, the Demo Code is shipped with the battery modes DISABLED. When the battery modes are disabled, the MPU will be halted once it enters brownout mode, even when a battery is present. See section 1.10.2 for instruction on how to enable battery modes.

If the main power source (internal or external power supply) is removed while a battery is connected to JP8 as described above, and if the battery modes are enabled with header JP12, the 71M6531D/F automatically enters Brownout mode. The Demo Code will then automatically transition from Brownout mode to Sleep mode.

By pressing the pushbutton PB, the chip is temporarily brought back to LCD mode. After a few seconds in LCD mode, the chip returns to Sleep mode.

By pressing the RESET pushbutton while the chip is in Sleep mode, the chip will enter Brownout mode.

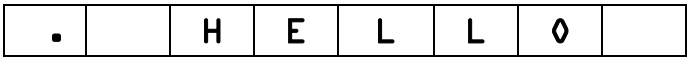
Both the RESET and PB buttons are powered by the battery voltage (VBAT).

In Brownout mode, the analog functions are disabled, and the MPU functions at very low speed. DIO pins and the UART are still functional. If the chip supports the command line interface, it will signal Brownout

mode, and the command prompt "B" will be visible on the terminal connected to the Demo Board, followed by the ">" sign:

B>

The LCD displays a decimal dot in the left-most digit to indicate that it is in Brownout mode, as shown below:



The following commands can be entered via the CLI in Brownout mode:

- BL – enters LCD mode
- BS – enters Sleep mode.
- BWSn – enters sleep mode for n seconds, then returns to Brownout mode
- BWMm – enters sleep mode for m minutes, then returns to Brownout mode

In Sleep Mode, almost all functions are disabled. Only the RTC and the wakeup timer are still active. The wakeup signal from the timer and the pushbutton (SW2 on the Demo Board) take the 71M6531D/F back to Brownout mode.

A hardware reset, while in any battery mode, takes the 71M6531D/F back to Brownout mode.

1.8 USING THE DEMO BOARD FOR METERING FUNCTIONS

1.8.1 MODIFYING DEMO CODE TO CT OR SHUNT MODE

Script files contained in the CD-ROM shipped with the Demo Kit can be used to modify the constants used in the Demo Code from CT to shunt mode or vice versa. Three script files are available:

1. **6531ctct.txt** sets 6531 Demo Code for IA: 2000:1 CT (Imax = 208A) and IB: 2000:1 CT (ImaxB = 208A)

2. **6531ctshunt.txt**: IA: 2000:1 CT (Imax = 208A) IB: 400 µΩ shunt (ImaxB = 442A)

3. **6531shuntct.txt**: IA: 400 µΩ shunt (Imax = 442A) IB: 2000:1 CT (ImaxB = 208A)

To apply a script file, select "transfer -> send_text_file" from the HyperTerminal user interface.

1.8.2 USING THE DEMO BOARD IN SHUNT AND CT MODES

The Demo Board may be used with current shunt sensors of 400µΩ resistance or current transformers (CTs). It is programmable for a Kh factor of 1.0 and (see Section 0 for adjusting the Demo Board for current transformers). Section 1.8.6 describes proper wiring and safety precautions for shunt operation.

Once, voltage is applied and load current is flowing, the red LED D5 will flash each time an energy sum of 1.0 Wh is collected. The LCD display will show the accumulated energy in Wh when set to display mode 3 (command >**M3** via the serial interface).

Similarly, the red LED D6 will flash each time an energy sum of 1.0 VARh is collected. The LCD display will show the accumulated energy in VARh when set to display mode 5 (command >**M5** via the serial interface).

The D6531N12A2 Demo Boards can be operated with CTs on channel B, which is equipped with the proper burden resistors for 2000:1 CTs.

If desired, channel A can be modified for operation with a 2000:1 CT as follows:

1) Remove R24 and R25. Insert a 1.7Ω resistor each for R24 and for R25.
2) Connect the output of the CT to terminal J3 on the bottom of the board.
3) Using the command line interface, change *IMAXA* to decimal 2080 (**>)A=+2080**) and *WRATE* to 1556 (**>]21=+1556**)
4) Remove R88, install L12 and L9.

Using the command line interface, change *IMAXA* and *WRATE* by sending the text file as described in 1.8.1. Of course, other winding ratios for CTs are possible. Adjusting the board to any CT winding ratio is described in 1.8.4.

If desired, channel A can be modified for operation with a shunt resistor as follows:

1) Remove R24 and R25. Insert a 10kΩ resistor for R24.
2) Install R88, remove L12 and L9.
3) Connect the shunt resistor wiring harness as shown in Figure 1-7.

Using the command line interface, change *IMAXA* and *WRATE* by sending the text file as described in 1.8.1.

1.8.3 ADJUSTING THE KH FACTOR FOR THE DEMO BOARD

The 71M6531 Demo Board is shipped with a pre-programmed scaling factor Kh of 1.0, i.e. 1.0 Wh per pulse. In order to be used with a calibrated load or a meter calibration system, the board should be connected to the AC power source using the spade terminals on the bottom of the board. The current transformer or shunt resistor should be connected to the dual-pin headers on the bottom of the board.

The Kh value can be derived by reading the values for IMAX and VMAX (i.e. the RMS current and voltage values that correspond to the 250mV maximum input signal to the IC), and inserting them in the following equation for Kh:

$$Kh = IMAX * VMAX * 47.1132 / (In\_8 * WRATE * N_{ACC} * X) = 0.99967 \text{ Wh/pulse.}$$

Where *IMAX* is the current scaling factor, *VMAX* is the voltage scaling factor, *In_8* is the current shunt gain factor, *WRATE* is the CE variable controlling Kh, N_{ACC} is the product of the I/O RAM registers *PRE_SAMPS* and *SUM_CYCLES*, and X is the pulse frequency factor derived from the CE variables *PULSE_SLOW* and *PULSE_FAST*.

The small deviation between the adjusted Kh of 0.99967 and the ideal Kh of 1.0 is covered by calibration. The default values used for the 71M6531 Demo Board are:

WRATE:	826
IMAX:	442
VMAX:	600
In_8:	1
N_{ACC}:	2520
X:	6

Explanation of factors used in the Kh calculation:

WRATE:	The factor input by the user to determine Kh
IMAX:	The current input scaling factor, i.e. the input current generating 176.8mVrms at the IA, IB, or IC input pins of the 71M6531D/F. 176.8mV rms is equivalent to 250mV peak.
VMAX:	The voltage input scaling factor, i.e. the voltage generating 176.8mVrms at the VA/VB/VC input pins of the 71M6531D/F
In_8:	The setting for the additional computational gain (8 or 1) determined by the CE register *IA_SHUNT*
N_{ACC}:	The number of samples per accumulation interval, i.e. *PRE_SAMPS *SUM_CYCLES*
X:	The pulse rate control factor determined by the CE registers *PULSE_SLOW* and *PULSE_FAST*

Almost any desired Kh factor can be selected for the Demo Board by resolving the formula for *WRATE*:

$$WRATE = (IMAX * VMAX * 47.1132) / (Kh * In\_8 * N_{ACC} * X)$$

For the Kh of 1.0Wh, the value 826 (decimal) should be entered for *WRATE* at location 0x21 (using the CLI command >**]21=+826**).

1.8.4 ADJUSTING THE DEMO BOARDS TO DIFFERENT CT WINDING RATIOS

In general, when *IMAX* is applied to the primary side of the CT, the voltage V_{in} at the IA or IB input of the 71M6531D/F IC is determined by the following formula:

$V_{in} = R * I = R * IMAX/N$
where N = transformer winding ratio, R = resistor on the secondary side (burden resistor)

If, for example, *IMAX* = 208A are applied to a CT with a 2500:1 ratio, only 83.2mA will be generated on the secondary side, causing only 141mV. In this case the Demo Board can be adapted with the steps outlined below:

1) The formula $R_x = \frac{176.8mV}{IMAX/N}$ is applied to calculate the new resistor R_x. We calculate R_x to 2.115Ω
2) **Changing the resistors R24/R25 or R106/R107 to a combined resistance of 2.115Ω** (for each pair) will cause the desired voltage drop of 176.8mV appearing at the IA, or IB inputs of the 71M6531D/F IC.
3) *WRATE* should be adjusted to achieve the desired Kh factor, as described in 1.8.3.

Simply scaling *IMAX* is not recommended, since peak voltages at the 71M6531D/F inputs should always be in the range of 0 through ±250mV (equivalent to 176.8mV rms). If a CT with a much lower winding ratio than 1:2,000 is used, higher secondary currents will result, causing excessive voltages at the 71M6531D/F inputs. Conversely, CTs with much higher ratio will tend to decrease the useable signal voltage range at the 71M6531D/F inputs and may thus decrease resolution.

1.8.5 ADJUSTING THE DEMO BOARDS TO VOLTAGE TRANSFORMERS OR DIFFERENT VOLTAGE DIVIDERS

The 71M6531 Demo Board comes equipped with its own network of resistor dividers for voltage measurement mounted on the PCB. The resistor values result in a ratio of 1:3,393.933. This means that *VMAX* equals 276.78mV*3,393.933 = 600V. A large value for *VMAX* has been selected in order to have headroom for overvoltages. This choice need not be of concern, since the ADC in the 71M6531D/F has enough resolution, even when operating at 120Vrms or 240Vrms.

If a **different set of voltage dividers** or an external voltage transformer is to be used, scaling techniques similar to those applied for the current transformer should be used.

In the following example we assume that the line voltage is not applied to the resistor divider for VA formed by R15-R21, R26-R31, and R32, but to a voltage transformer with a ratio N of 20:1, followed by a simple resistor divider. We also assume that we want to maintain the value for *VMAX* at 600V to provide headroom for large voltage excursions.

When applying *VMAX* at the primary side of the transformer, the secondary voltage V_s is:

$V_s = VMAX / N$

V_s is scaled by the resistor divider ratio R_R. When the input voltage to the voltage channel of the 71M6531D/F is the desired 176.8mV, V_s is then given by:

$V_s = R_R * 176.8mV$

Resolving for R_R, we get:

$R_R = (VMAX / N) / 176.8mV = (600V / 30) / 176.8mV = 170.45$

This divider ratio can be implemented, for example, with a combination of one 16.95kΩ and one 100Ω resistor.

1.8.6 WIRING OF THE DEMO BOARD AND A SHUNT RESISTOR

The 71M6531 Demo Kits are shipped with a pre-wired shunt resistor (400µΩ), as shown in Figure 1-6. This shunt resistor has to be connected to the 71M6531 Demo Board, as shown in Figure 1-7.

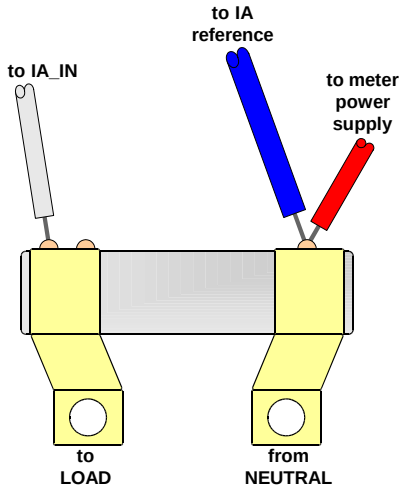


Figure 1-6: Pre-wired shunt resistor

Important safety precautions apply when operating the Demo Board in shunt mode:

In shunt configuration, the whole Demo Board will be at line voltage! Touching the board or any components must be avoided!

It is highly recommended to isolate Demo Board and Debug Board (when used) and to provide separate power supplies for the Demo Board and Debug Board.

Emulators or other test equipment should never be connected to a live meter without proper isolation!

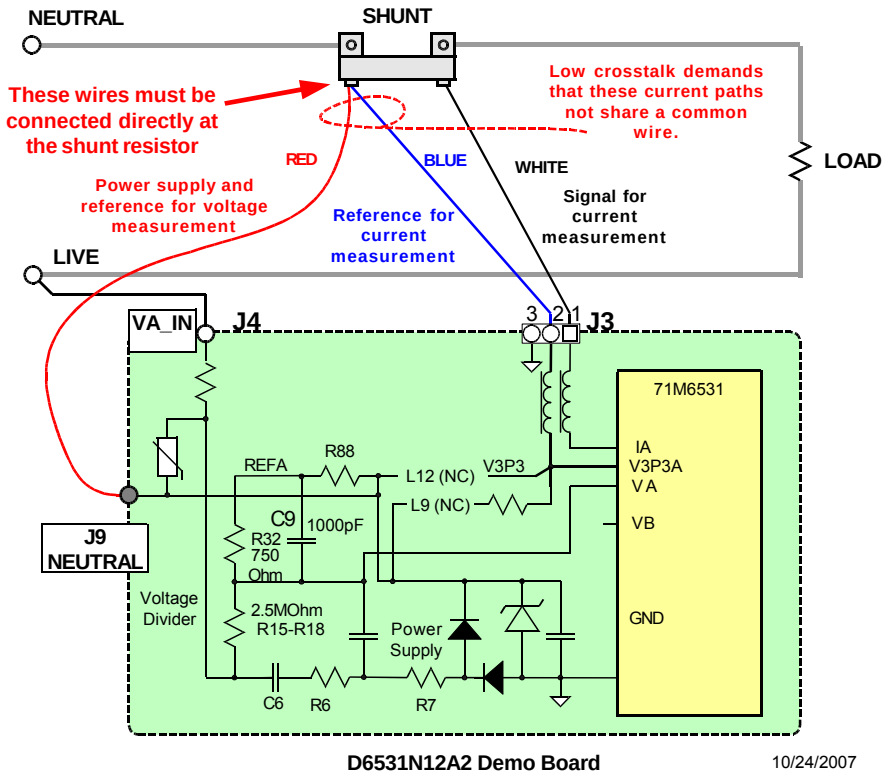


Figure 1-7: Connection of the Pre-Wired Shunt Resistor

While connecting wires to J9 and J4, care should be taken to prevent shorting between LINE and NEUTRAL.

Before connecting the Demo Board to main power, the resistance between J9 and J4 (LIVE and NEUTRAL) must be checked! If the resistance is below 100Ω, the wiring must be re-checked!

Only one shunt resistor can be used in a meter, since isolation cannot be maintained when using more than one shunt resistor.

1.9 CALIBRATION PARAMETERS

1.9.1 GENERAL CALIBRATION PROCEDURE

Any calibration method can be used with the 71M6531D/F chips. This Demo Board User's Manual presents calibration methods with three or five measurements as recommended methods, because they work with most manual calibration systems based on counting "pulses" (emitted by LEDs on the meter).

Naturally, a meter in mass production will be equipped with special calibration code offering capabilities beyond those of the Demo Code. It is basically possible to calibrate using voltage and current readings, with or without pulses involved. For this purpose, the MPU Demo Code can be modified to display averaged voltage and current values (as opposed to momentary values). Also, automated calibration equipment can communicate with the Demo Boards via the serial interface and extract voltage and current readings. This is possible even with the unmodified Demo Code.

A complete calibration procedure is given in section 2.1.3 of this manual.

Regardless of the calibration procedure used, parameters (calibration constants) will result that will have to be applied to the 71M6531D/F chip in order to make the chip apply the modified gains and phase shifts necessary for accurate operation. Table 1-10 shows the names of the calibration constants, their function, and their location in the XRAM.

Again, the command line interface can be used to store the calibration constants in their respective XRAM addresses. For example, the command

```
>]11=+16302
```

stores the decimal value 16302 in the XRAM location controlling the gain of the voltage channel (*CAL_VA*).

Constant	CE Address (hex)	Description
CAL_VA *CAL_VB*	0x11 0x13	Adjusts the gain of the voltage channel. +16384 is the typical value. The gain is directly proportional to the CAL parameter. Allowed range is 0 to 32767. If the gain is 1% slow, CAL should be increased by 1%.
CAL_IA *CAL_IB*	0x10 0x12	Adjusts the gain of the current channels. +16384 is the typical value. The gain is directly proportional to the CAL parameter. Allowed range is 0 to 32767. If the gain is 1% slow, CAL should be increased by 1%.
PHADJ_A *PHADJ_B*	0x18 0x19	This constant controls the CT phase compensation. No compensation occurs when *PHADJ* = 0. As *PHADJ* is increased, more compensation is introduced. **Note: *PHADJ_B* [1] applies to 3W/1-phase systems.**

Table 1-10: XRAM Locations for Calibration Constants

1.9.2 UPDATING THE 6531_DEMO.HEX FILE

The d_merge program updates the 6531_demo.hex file with the values contained in the macro file. This program is executed from a DOS command line window. Executing the d_merge program with no arguments will display the syntax description. To merge macro.txt and old_6531_demo.hex into new_6531_demo.hex, use the command:

```
d_merge old_6531_demo.hex macro.txt new_6531_demo.hex
```

The new hex file can be written to the 71M6531D/F through the ICE port using the ADM51 in-circuit emulator. This step makes the calibration to the meter permanent.

1.9.3 CALIBRATION MACRO FILE

The macro file in Figure 1-8 contains a sequence of commands to be used for Demo Boards that provide a serial command line interface (CLI). It is a simple text file and can be created with Notepad or an equivalent ASCII editor program. The file is executed with HyperTerminal's *Transfer->Send Text File* command.

```
]10=+16022/ CAL_IA (gain=CAL_IA/16384)
]11=+16381/ CAL_VA (gain=CAL_VA/16384)
]12=+16019/ CAL_IB (gain=CAL_IB/16384)
]13=+16370/ CAL_VB (gain=CAL_VB/16384)
]18=+115/   PHADJ_A (default 0)
]19=+113/   PHADJ_B (default 0)
ce1
```

Figure 1-8: Typical Calibration Macro file

It is possible to send the calibration macro file to the 71M6531D/F for "temporary" calibration. This will temporarily change the CE data values. Upon power up, these values are refreshed back to the default values stored in flash memory. Thus, until the flash memory is updated, the macro file must be loaded each time the part is powered up. The macro file is run by first issuing the ce0 command to turn off the compute engine and then sending the file with the *transfer → send text file* procedure. Turning off the CE before changing CE constants is not a hardware requirement of the chip, but is recommended because of the way the demo code is written.

Note: Do not use the *Transfer → Send File* command!

1.9.4 UPDATING CALIBRATION DATA IN EEPROM OR FLASH

It is possible to make data permanent that had been entered temporarily into the XRAM. The transfer to EEPROM is done using the following serial interface command:

```
>CLS
```

Thus, after transferring calibration data with manual serial interface commands or with a macro file, all that has to be done is invoking the **CLS** command.

It is also possible to write calibration data to flash memory. This is done using the following serial interface command:

```
>]U
```

1.9.5 LOADING THE 6531_DEMO.HEX FILE INTO THE DEMO BOARD

Hardware Interface for Programming: The 71M6531D/F IC provides an interface for loading code into the internal flash memory. This interface consists of the following signals:

E_RXTX (data), E_TCLK (clock), E_RST (reset), ICE_E (ICE enable)

These signals, along with V3P3D and GND are available on the emulator header J14. Production meters may be equipped with much simpler programming connectors, e.g. a 6x1 header.

Programming of the flash memory requires a specific in-circuit emulator, the ADM51 by Signum Systems (http//www.signumsystems.com) or the Flash Programmer (TFP-2) provided by TERIDIAN Semiconductor.

Chips may also be programmed before they are soldered to the board. The TGP1 gang programmer suitable for high-volume production is available from TERIDIAN.

In-Circuit Emulator: If firmware exists in the 71M6531D/F flash memory, this memory has to be erased before loading a new file into memory. Figure 1-9 and Figure 1-10 show the emulator software active. In order to erase the flash memory, the RESET button of the emulator software graphical interface has to be clicked followed by the ERASE button (Figure 1-9).

Once the flash memory is erased, the new file can be loaded using the commands File followed by Load. The dialog box shown in Figure 1-10 will then appear making it possible to select the file to be loaded by clicking the Browse button. Once the file is selected, pressing the OK button will load the file into the flash memory of the 71M6531D/F IC.

At this point, the emulator probe (cable) can be removed. Once the 71M6531D/F IC is reset using the reset button on the Demo Board, the new code starts executing.

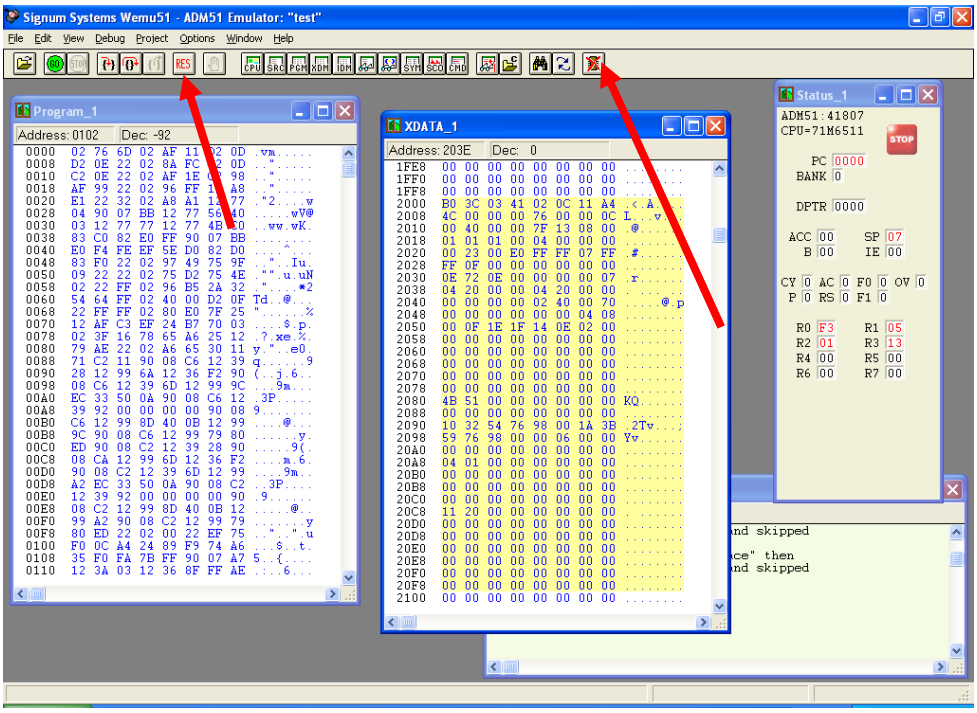


Figure 1-9: Emulator Window Showing Reset and Erase Buttons

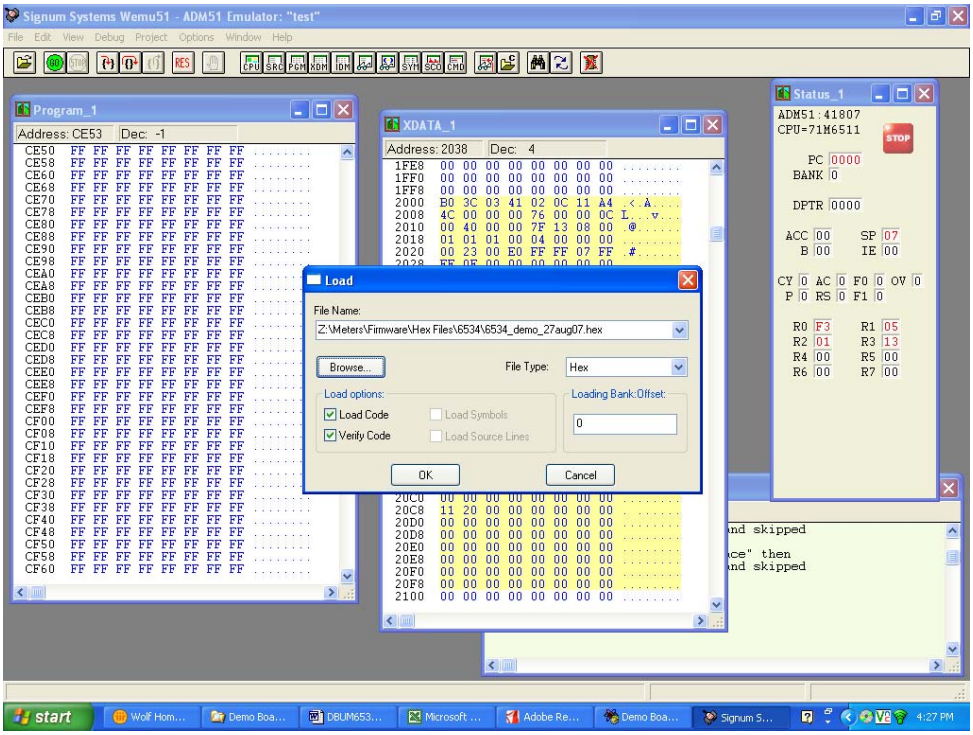


Figure 1-10: Emulator Window Showing Erased Flash Memory and File Load Menu

Flash Downloader Module (TFP-2): Follow the instructions given in the User Manual for the TFP-2.

Emulators or other test equipment should never be connected to a live meter without proper isolation! USB isolators are available from various vendors (see the printed Safety Notice shipped with the emulator).

1.9.6 THE PROGRAMMING INTERFACE OF THE 71M6531D/F

TFP-2 and ICE Interface Signals

The signals listed in Table 1-11 are necessary for communication between the Flash Programmer or ICE and the 71M6531D/F.

Signal	Direction	Function	Available on
E_TCLK	Output from 71M6531D/F	Data clock	ICE, TFP-2
E_RXTX	Bi-directional	Data input/output	ICE, TFP-2
E_RST	Bi-directional	Flash Downloader Reset (active low)	ICE, TFP-2
ICE_ENA	Input of 71M6531D/F	Enables ICE interface	TFP-2

Table 1-11: Flash Programming Interface Signals

The E_RST signal should only be driven by the ICE or Flash Downloader when enabling the ICE interface. E_RST must be floating at all other times.

The same hardware and software precautions mentioned for emulator (ICE) operation in section 1.11 apply to Flash Programmer operation.

1.10 DEMO CODE

1.10.1 DEMO CODE DESCRIPTION

The Demo Board is shipped preloaded with Demo Code revision 4p6q or later in the 71M6531D/F chip. The code revision can easily be verified by entering the command **>i** via the serial interface (see section 1.7.2). Check with your local TERIDIAN representative or FAE for the latest revision.

Firmware for the Demo Boards can be updated using either an in-circuit emulator (ICE) or the Flash Programmer (TFP-2), as described in section 1.9.5.

The Demo Code is useful due to the following features:

- It provides basic metering functions such as pulse generation, display of accumulated energy, frequency, date/time, and enables the user to evaluate the parameters of the metering IC such as accuracy, harmonic performance, etc.
- It maintains and provides access to basic household functions such as real-time clock (RTC).
- It provides access to control and display functions via the serial interface, enabling the user to view and modify a variety of meter parameters such as Kh, calibration coefficients, temperature compensation etc.
- It provides libraries for access of low-level IC functions to serve as building blocks for code development.

The Demo Code source files provided with the TERIDIAN Demo Kits contain numerous routines that are not implemented. However, by recompiling the code using different compile-time options, many code variations with different features can be generated. See the Software User's Guide (SUG) for a complete description of the Demo Code.

1.10.2 ACCESSING LCD AND SLEEP MODES FROM BROWNOUT MODE

Header JP12 controls the behavior of the Demo Code when system power is off. The setting of JP12 is read on power up (or after reset), and controls the Demo Code as follows:

- Jumper across pins 1-2 (GND): The Demo Code will communicate at 9600bd. No transitions to sleep or LCD mode will be made from brownout mode.
- Jumper across pins 2-3 (V3P3): The Demo Code will communicate at 300bd. Transitions to sleep or LCD mode can be made from brownout mode. **This operation mode requires connection of a battery or equivalent DC voltage at JP8.**

1.10.3 DEMO CODE MEMORY LOCATIONS

Registers in MPU data RAM can be accessed via the command line interface (CLI) or the using the method involving Intel Hex records.

Table 1-12 lists MPU addresses of interest. Manipulating the values in the MPU addresses enables the user to change the behavior of the meter. For example, if the current transformer external to the Demo Board is changed, a different *IMAX* value n may have to be applied. This can be done by changing the value in the address for *IMAX* using the CLI command **)<addess>=n**. Modifications to MPU data RAM will not be maintained when a reset or power-up occurs.

Changes to the MPU data RAM can be made permanent by creating a macro file containing one or several CLI commands and merging the macro file into the code using the d_merge utility described in section 1.9.2.

The following is an example showing how the battery bit can be set permanently by creating a new object file:

A text file (battery.txt) is generated, containing the CLI command **)1=20**. The d_merge utility is called, using the following syntax (**6531_demo.hex** is the existing object file):

```
d_merge 6531_demo.hex battery.txt new_6531_demo.hex
```

Now, the object file **new_6531_demo.hex** contains the battery bit.

Name	Purpose	Function or LSB Value	CLI	F	L in bits	XDATA
IThrshldA	Starting current, element A	$LSB = 2^{16}\sqrt{I0SQSUM}$ 0 in this position disables creep logic for both element A and B.	)0	U	32	0x0000
Config	Configure meter operation on the fly.	bit 0:** reserved 0: VA = Vrms * Irms; 1: $VA = \sqrt{Wh^2 + VARh^2}$ bit1: 1 = Clears accumulators bit2:1 = Calibration mode bit3:** reserved: 1 = enable tamper detection **bit 5: 1 = battery modes enabled**	)1	N/A	8	0x0004
VPThrshld	error if exceeded.	$LSB = 2^{16}\sqrt{V0SQSUM}$	)2	U	32	0x0005
IPThrshld	error if exceeded.	$LSB = 2^{16}\sqrt{I0SQSUM}$	)3	U	32	0x0009
Y_Cal_Deg0	RTC adjust, provided for optional code.	100ppb	)4	S	16	0x000D
Y_Cal_Deg1	RTC adjust, linear by temp.	10ppb*ΔT, in 0.1˚C	)5	S	16	0x000F
Y_Cal_Deg2	RTC adjust, squared by temp.	1ppb*ΔT^2, in 0.1˚C	)6	S	16	0x0011
PulseWSource *PulseVSource*	Wh Pulse source, VARh pulse source selection	See table for PulseWSource and PulseVSource	)7)8	U	8	0x0013 0x0014
Vmax	Scaling Maximum Voltage for PCB, equivalent to 176mV at the VA/VB pins	0.1V	)9	U	16	0x0015
ImaxA	Scaling maximum current for element A, equivalent to 176mV at the IA pin	0.1A	)A	U	16	0x0017
ppmc1	ADC linear adjust with temperature	PPM per degree centigrade	)B	S	16	0x0019
ppmc2	ADC quadratic adjust with temperature	PPM per degree centigrade squared	)C	S	16	0x001B
Pulse 3 source	Source for software pulse output 3	See table for *PulseWSource* and *PulseVSource*	)D	U	8	0x001D
Pulse 4 source	Source for software pulse output 4	See table for *PulseWSource* and *PulseVSource*	)E	U	8	0x001E
Scal	Duration for auto-calibration in seconds	Count of accumulation intervals to be used for auto-calibration.	)F	U	16	0x001F
Vcal	Voltage value to be used for auto-calibration	Nominal RMS voltage applied to all elements during auto-calibration (LSB = 0.1V).	)10	U	16	0x0021

Name	Purpose	Function or LSB Value	CLI	For mat	L in bits	XDATA
Ical	Current value to be used for autocalibration	Nominal RMS current applied to all elements during auto-calibration (LSB = 0.1V). Power factor must be 1.	)11	U	16	0x0023
VThrshld	Voltage at which to measure frequency, zero crossing, etc.	$LSB = 2^{16}\sqrt{V0SQSUM}$ This feature is approximated using the CE's sag detection.)	)12	U	16	0x0025
PulseWidth	Maximum time pulse is on.	t = (2*PulseWidth + 1)*397µs, 0xFF disables this feature. Takes effect only at start-up.	)13	S	16	0x0029
TEMP_NOM	Nominal temperature, the temperature at which calibration occurs.	Units of *TEMP_RAW*, from CE. The value read from the CE must be entered at this address.	)14	U	32	0x002B
ImaxB	Scaling maximum current for element B, equivalent to 176mV at the IA pin	0.1A	)15	U	16	0x002F
IThrshldB	Starting current, element B	$2^{16}\sqrt{I1SQSUM}$	)16	U	32	0x0031
VBatMin	Minimum battery voltage.	Same as VBAT, below	)17	U	32	0x0035
CalCount	Count of calibrations	Counts the number of times calibration is saved, to a maximum of 255	)18	U	8	0x0039
RTC copy	Nonvolatile copy of the most recent time the RTC was read.	Sec, Min, Hr, Day, Date, Month, Year	)19)1A)1B)1C)1D)1E)1F	U	8 8 8 8 8 8 8	0x017A 0x017B 0x017C 0x017D 0x017E 0x017F 0x0180
deltaT	Difference between raw temperature and temp_nom	Same units as *TEMP_RAW*	)20	S	32	0x003C
Frequency	Frequency	Units from CE.	)21	U	32	0x0040
*VBAT**	Last measured battery voltage	$VBAT = \frac{n_{ADC}}{2^9}$ ADC counts, logically shifted right by 9 bits. Note: battery voltage is measured once per day, except when it is being displayed or requested with the BT command.	)22	U	32	0x0044

Name	Purpose	Function or LSB Value	CLI	F	L in bits	XDATA
Vrms_A	Vrms, element A	$2^{16}\sqrt{V0SQSUM}$	)24	U	32	0x004C
Irms_A	Irms, element A	$2^{16}\sqrt{I0SQSUM}$	)25	U	32	0x0050
Vrms_B	Vrms, element B	$2^{16}\sqrt{V1SQSUM}$	)26	U	32	0x0054
Irms_B	Irms, element B	$2^{16}\sqrt{I1SQSUM}$	)27	U	32	0x0058
Vrms_C	(reserved)		)28	U	32	0x005C
Irms_C	(reserved)		)29	U	32	0x0060
STATUS	Status of meter	See table for *STATUS* register	)2A	U	32	0x0064
CAI	Count of accumulation intervals since reset, or last clear.	count	)2B	S	32	0x0068
*Whi***	Imported Wh, all elements.	Same LSB as *W0SUM*	)2C	S	64	0x006C
*Whi_A***	Imported Wh, element A	"	)2E	S	64	0x0074
*Whi_B***	Imported Wh, element B	"	)30	S	64	0x007C
*Whi_C***	(reserved)		)32	S	64	0x0084
*VARhi**	Imported VARh, all elements.	LSB of *W0SUM*	)34	S	64	0x008C
*VARhi_A**	Imported VARh, element A	"	)36	S	64	0x0094
*VARhi_B**	Imported VARh, element B	"	)38	S	64	0x009C
*VARhi_C**	(reserved)		)3A	S	64	0x00A4
*VAh***	VAh, all elements.	LSB of *W0SUM*	)3C	S	64	0x00AC
*VAh_A***	VAh, element A	"	)3E	S	64	0x00B4
*VAh_B***	VAh, element B	"	)40	S	64	0x00BC
*VAh_C***	(reserved)		)42	S	64	0x00C4
*Whe***	Exported Wh, all elements.	LSB of *W0SUM*	)44	S	64	0x00CC
*Whe_A***	Exported Wh, element A	"	)46	S	64	0x00D4
*Whe_B***	Exported Wh, element B	"	)48	S	64	0x00DC
*Whe_C***	(reserved)		)4A	S	64	0x00E4

Name	Purpose	Function or LSB Value	CLI	F	L in bits	XDATA
VARhe	Exported VARh, all elements.	LSB of *W0SUM*	)4C	S	64	0x00EC
VARhe_A	Exported VARh, element A	"	)4E	S	64	0x00F4
VARhe_B	Exported VARh, element B	"	)50	S	64	0x00FC
VARhe_C	(reserved)		)52	S	64	0x0104
Whn	Net metered Wh, all elements A,	LSB of *W0SUM*	)54	S	64	0x010C
Whn_A	Net metered Wh, element A, for autocalibration	LSB of *W0SUM*	)56	S	64	0x0114
Whn_B	Net metered Wh, element B	"	)58	S	64	0x011C
Whn_C	(reserved)		)5A	S	64	0x0124
VARhn	Net metered VARh, all elements	LSB of *W0SUM*	)5C	S	64	0x012C
VARhn_A	Net metered VARh, element A, for auto-calibration	"	)5E	S	64	0x0134
VARhn_B	Net metered VARh, element B	"	)60	S	64	0x013C
VARhn_C	(reserved)		)62	S	64	0x0144
MainEdgeCnt	Count of voltage zero crossings	count	)64	U	32	0x014C
Wh	Default sum of Wh, nonvolatile	LSB of *W0SUM*	)65	S	64	0x0150
Wh_A	Wh, element A, nonvolatile	"	)67	S	64	0x0158
Wh_B	Wh, element B, nonvolatile	"	)69	S	64	0x0160
Wh_C	(reserved)		)6B	S	64	0x0164
StatusNV	Nonvolatile status	See Status	)6D	n/a	32	0x0170

Table 1-12: MPU memory locations

Table 1-13 lists the possible entries for the PULSEWSOURCE and PULSEVSOURCE registers.

Decimal Value in PULSEWSOURCE, PULSEVSOURCE	Selected Pulse Source	Decimal Value in PULSEWSOURCE, PULSEVSOURCE	Selected Pulse Source
0	EQU= 0: *W0SUM* if *W0SUM* > *W1SUM*, *W1SUM* if *W1SUM* > *W0SUM***	18	(reserved)
1	*W0SUM*	19	*WSUM_I*
2	*W1SUM*	20	*W0SUM_I*
3	(reserved)	21	*W1SUM_1*
4	*VARSUM*	22	(reserved)
5	*VAR0SUM*	23	*VARSUM_I*
6	*VAR1SUM*	24	*VAR0SUM_I*
7	(reserved)	25	*VAR1SUM_I*
8	*I0SQSUM*	26	(reserved)
9	*I1SQSUM*	27	*WSUM_E*
10	(reserved)	28	*W0SUM_E*
11	*INSQSUM*	29	*W1SUM_E*
12	*V0SQSUM*	30	(reserved)
13	*V1SQSUM*	31	*VARSUM_E*
14	(reserved)	32	*VAR0SUM_E*
15	*VASUM*	33	*VAR1SUM_E*
16	*VA0SUM*	34	(reserved)
17	*VA1SUM*		

*****Changing the equation (EQU) in the I/O RAM does not alter the computations implemented in the Demo Code.**

Table 1-13: Values for Pulse Source Registers

Table 1-14 explains the bits of the *STATUS* register.

Bit	Significance	Bit	Significance
0	CREEP: All elements are in creep mode. The pulse variables will be "jammed" with a constant value on every accumulation interval to prevent spurious pulses. Therefore, creep mode stops pulsing even in internal pulse mode.	16	BATTERY_BAD: The battery voltage is below VBatMin. The battery is checked only once per day, right after midnight.
1	--	17	--
2	PB_PRESS: An activation of the pushbutton was recorded at the most recent reset or wake from battery mode.	18	CAL_BAD: This bit is set after reset if the longitudinal checksum over calibration factors is invalid.
3	WAKE_ALARM: An wake timer flag was recorded at the most recent wake from battery mode.	19	CLOCK_UNSET: This bit is set after reset if is determined that the RTC has never been set, indicating a bad or non-existent battery.
4	MINVB: Voltage at element B is below VThrshld. The element is in creep mode.	20	POWER_BAD: This bit is set after reset if is determined that both longitudinal checksums over the two sets of energy billing data are bad.
5	MAXVA: Voltage at element A is above VThrshldP.	21	GNDNEUTRAL: This bit indicates that a grounded neutral was detected.
6	MAXVB: Voltage at element B is above VThrshldP.	22	TAMPER: This bit indicates that a tampering attempt was detected (compilation option, not supported on standard Demo Board).
7	--	23	VXEDGE: Copy of the CE MAIN_EDGE bit.
8	MINVA: Voltage at element A is below VThrshld. The element is in creep mode.	24	--
9	WD_DETECT: The most recent reset was caused by the WDT	25	SAGA: Copy of the CE SAG_A bit w/ a maximum delay of 8 sample intervals.
10	--	26	SAGB: Copy of the CE SAG_B bit
11	MAXIA: The current in element A is above IThrshld	27	--
12	MAXIB: The current in element B is above IThrshld	28	F0_CE: A copy of the F0 bit of the CE, with a jitter of up to 8 sample intervals.
13	--	29	--
14	MINT: The temperature is below the minimum (as defined in option_gbl.h)	30	--
15	MAXT: The temperature is above the maximum (as defined in option_gbl.h)	31	ONE_SEC: This bit changes every accumulation interval.

Table 1-14: *STATUS* register

MPU ACCUMULATION OUTPUT VARIABLES

Accumulation values are accumulated from XFER cycle to XFER cycle (see Table 1-15). They are organized as two 32-bit registers. The first register stores the decimal number displayed on the LCD. For example, if the LCD shows "001.004", the value in the first register is 1004. This register wraps around after the value 999999 is reached. The second register holds fractions of the accumulated energy, with an LSB of $9.4045*10^{-13}$*VMAX*IMAX*In_8 Wh.

The MPU accumulation registers always hold positive values.

The CLI commands with two question marks, e.g. **)39??** should be used to read the variables.

XRAM Word Address	Name	Description
0x2C	*Whi*	Total Watt hours consumed (imported)
0x44	*Whe*	Total Watt hours generated (exported)
0x34	*VARhi*	Total VAR hours consumed
0x4C	*VARhe*	Total VAR hours generated (inverse consumed)
0x3C	*VAh*	Total VA hours
0x2E	*Whi_A*	Total Watt hours consumed through element 0
0x46	*Whe_A*	Total Watt hours generated (inverse consumed) through element 0
0x36	*VARhi_A*	Total VAR hours consumed through element 0
0x4E	*VARhe_A*	Total VAR hours generated (inverse consumed) through element 0
0x3E	*VAh_A*	Total VA hours in element 0
0x30	*Whi_B*	Total Watt hours consumed through element 1
0x48	*Whe_B*	Total Watt hours generated (inverse consumed) through element 1
0x38	*VARhi_B*	Total VAR hours consumed through element 1
0x50	*VARhe_B*	Total VAR hours generated (inverse consumed) through element 1
0x40	*Vah_B*	Total VA hours in element 1

Table 1-15: MPU Accumulation Output Variables

1.11 EMULATOR OPERATION

The Signum Systems ADM51 ICE (In-Circuit-Emulator) can be plugged into J14 (or J15) of the Demo Board. The following conditions are required for successful emulator operation (including code load/erase in flash memory):

1) Emulator operation is enabled by plugging a jumper into header JP4, pins V3P3D/ICE_E
2) The CE is disabled (using serial command **CE0** or writing 0x00 to I/O RAM cell 0x2000)

For details on code development and test see the Software User's Guide (SUG).

The emulator can also be operated when the 71M6531D/F is in brownout mode. In brownout mode, the 71M6531D/F provides power for the pull-up resistors necessary for emulator operation via its V3P3D pin.

Emulators or other test equipment should never be connected to a live meter without proper isolation! USB isolators are available from various vendors (see the printed Safety Notice shipped with the emulator).

2

2 APPLICATION INFORMATION

2.1 CALIBRATION THEORY

A typical meter has phase and gain errors as shown by ϕ_S, A_{XI}, and A_{XV} in Figure 2-1. Following the typical meter convention of current phase being in the lag direction, the small amount of phase lead in a typical current sensor is represented as $-\phi_S$. The errors shown in Figure 2-1 represent the sum of all gain and phase errors. They include errors in voltage attenuators, current sensors, and in ADC gains. In other words, no errors are made in the 'input' or 'meter' boxes.

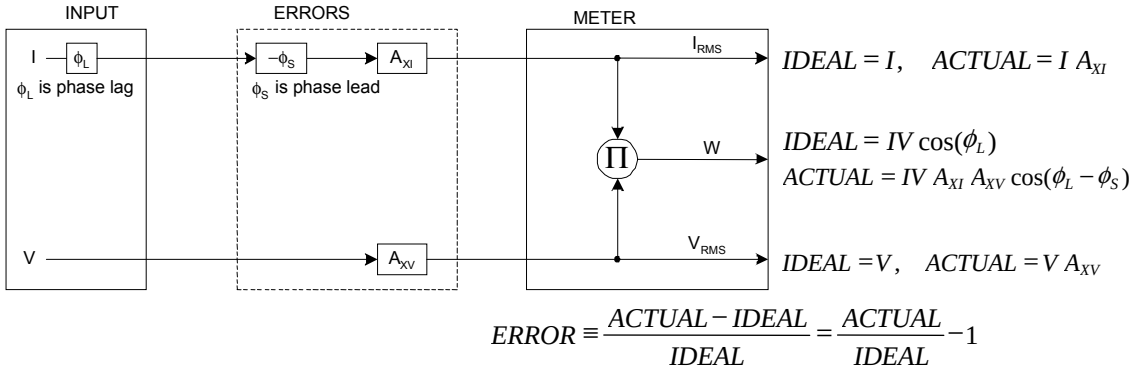


Figure 2-1: Watt Meter with Gain and Phase Errors.

During the calibration phase, we measure errors and then introduce correction factors to nullify their effect. With three unknowns to determine, we must make at least three measurements. If we make more measurements, we can average the results.

2.1.1 CALIBRATION WITH THREE MEASUREMENTS

A simple calibration method uses three measurements. Typically, a voltage measurement and two Watt-hour (Wh) measurements are made. A voltage display can be obtained for test purposes via the command >**MR2.1** in the serial interface.

Let's say the voltage measurement has the error E_V and the two Wh measurements have errors E_0 and E_{60}, where E_0 is measured with $\phi_L = 0$ and E_{60} is measured with $\phi_L = 60$. These values should be simple ratios—not percentage values. They should be zero when the meter is accurate and negative when the meter runs slow. The fundamental frequency is f_0. T is equal to $1/f_S$, where f_S is the sample frequency (2560.62Hz). Set all calibration factors to nominal: *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJA* = 0.

From the voltage measurement, we determine that

1.➔ $$A_{XV} = E_V + 1$$

We use the other two measurements to determine ϕ_S and A_{XI}.

2. $$E_0 = \frac{IV\, A_{XV}\, A_{XI} \cos(0 - \phi_S)}{IV \cos(0)} - 1 = A_{XV}\, A_{XI} \cos(\phi_S) - 1$$

2a. $$A_{XV} A_{XI} = \frac{E_0 + 1}{\cos(\phi_S)}$$

3. $$E_{60} = \frac{IV\, A_{XV}\, A_{XI} \cos(60 - \phi_S)}{IV \cos(60)} - 1 = A_{XV}\, A_{XI} \frac{\cos(60 - \phi_S)}{\cos(60)} - 1$$

3a. $$E_{60} = \frac{A_{XV} A_{XI} \left[\cos(60)\cos(\phi_S) + \sin(60)\sin(\phi_S)\right]}{\cos(60)} - 1$$

$$= A_{XV} A_{XI} \cos(\phi_S) + A_{XV} A_{XI} \tan(60)\sin(\phi_S) - 1$$

Combining 2a and 3a:

4. $$E_{60} = E_0 + (E_0 + 1)\tan(60)\tan(\phi_S)$$

5. $$\tan(\phi_S) = \frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}$$

6.➔ $$\phi_S = \tan^{-1}\left(\frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}\right)$$

and from 2a:

7.➔ $$A_{XI} = \frac{E_0 + 1}{A_{XV} \cos(\phi_S)}$$

Now that we know the A_{XV}, A_{XI}, and ϕ_S errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from ϕ_S, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1 + (1 - 2^{-9})^2 - 2(1 - 2^{-9})\cos(2\pi f_0 T)\right]}{(1 - 2^{-9})\sin(2\pi f_0 T) - \tan(\phi_S)\left[1 - (1 - 2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

And we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}} \frac{1}{\sqrt{1+\frac{2^{-20}\,PHADJ\,(2+2^{-20}\,PHADJ-2(1-2^{-9})\cos(2\pi f_0 T))}{1-2(1-2^{-9})\cos(2\pi f_0 T)+(1-2^{-9})^2}}}$$

2.1.2 CALIBRATION WITH FIVE MEASUREMENTS

The five measurement method provides more orthogonality between the gain and phase error derivations. This method involves measuring E_V, E_0, E_{180}, E_{60}, and E_{300}. Again, set all calibration factors to nominal, i.e. *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJA* = 0.

First, calculate A_{XV} from E_V:

1.➔ $$A_{XV} = E_V + 1$$

Calculate A_{XI} from E_0 and E_{180}:

2. $$E_0 = \frac{IV\,A_{XV}\,A_{XI}\cos(0-\phi_S)}{IV\cos(0)} - 1 = A_{XV}\,A_{XI}\cos(\phi_S) - 1$$

3. $$E_{180} = \frac{IV\,A_{XV}\,A_{XI}\cos(180-\phi_S)}{IV\cos(180)} - 1 = A_{XV}\,A_{XI}\cos(\phi_S) - 1$$

4. $$E_0 + E_{180} = 2A_{XV}A_{XI}\cos(\phi_S) - 2$$

5. $$A_{XV}A_{XI} = \frac{E_0 + E_{180} + 2}{2\cos(\phi_S)}$$

6.➔ $$A_{XI} = \frac{(E_0 + E_{180})/2 + 1}{A_{XV}\cos(\phi_S)}$$

Use above results along with E_{60} and E_{300} to calculate ϕ_S.

7. $$E_{60} = \frac{IV\,A_{XV}\,A_{XI}\cos(60-\phi_S)}{IV\cos(60)} - 1$$

$$= A_{XV}A_{XI}\cos(\phi_S) + A_{XV}A_{XI}\tan(60)\sin(\phi_S) - 1$$

8. $$E_{300} = \frac{IV\,A_{XV}\,A_{XI}\cos(-60-\phi_S)}{IV\cos(-60)} - 1$$

$$= A_{XV}A_{XI}\cos(\phi_S) - A_{XV}A_{XI}\tan(60)\sin(\phi_S) - 1$$

Subtract 8 from 7

9. $$E_{60} - E_{300} = 2A_{XV}A_{XI}\tan(60)\sin(\phi_S)$$

use equation 5:

10. $$E_{60} - E_{300} = \frac{E_0 + E_{180} + 2}{\cos(\phi_S)}\tan(60)\sin(\phi_S)$$

11. $$E_{60} - E_{300} = (E_0 + E_{180} + 2)\tan(60)\tan(\phi_S)$$

12.➔ $$\phi_S = \tan^{-1}\left(\frac{(E_{60} - E_{300})}{\tan(60)(E_0 + E_{180} + 2)}\right)$$

Now that we know the A_{XV}, A_{XI}, and ϕ_S errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from ϕ_S, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1+(1-2^{-9})^2 - 2(1-2^{-9})\cos(2\pi f_0 T)\right]}{(1-2^{-9})\sin(2\pi f_0 T) - \tan(\phi_S)\left[1-(1-2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

And we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}} \frac{1}{\sqrt{1+\frac{2^{-20}\,PHADJ\,(2+2^{-20}\,PHADJ - 2(1-2^{-9})\cos(2\pi f_0 T))}{1-2(1-2^{-9})\cos(2\pi f_0 T)+(1-2^{-9})^2}}}$$

2.1.3 FAST CALIBRATION

The calibration methods described so far require that the calibration system sequentially applies currents at various phase angles. A simpler approach is based on the calibration system applying a constant voltage and current at exactly zero degrees phase angle. This approach also requires much simpler mathematical operations.

Before starting the calibration process, the voltage and current calibration factors are set to unity (16384) and the phase compensation factors are set to zero.

During the calibration process, the meter measures for a given constant time, usually 30 seconds, and is then examined for its accumulated Wh and VARh energy values. Access to the internal accumulation registers is necessary for this method of calibration. The phase angle introduced by the voltage and/or current sensors is then simply determined by:

$$\varphi = a\tan\frac{VARh}{Wh}$$

CAL_VA is determined by comparing the applied voltage to the measured voltage, or:

$$CAL\_VA = 16384 \cdot \frac{V_{applied}}{V_{measured}}$$

CAL_IA is determined by comparing applied real energy with the measured apparent energy (and compensating for the change applied to *CAL_VA*):

$$CAL\_IA = \frac{16384 \cdot Wh_{applied}}{VAh_{measured} \cdot CAL\_VA} \cdot$$

The derivation of these formulae is shown in the Appendix.

2.2 CALIBRATION PROCEDURES

2.2.1 GENERAL PRECAUTIONS

Calibration requires that a calibration system is used, i.e. equipment that applies accurate voltage, load current and load angle to the unit being calibrated, while measuring the response from the unit being calibrated in a repeatable way. By repeatable we mean that the calibration system is synchronized to the meter being calibrated. Best results are achieved when the first pulse from the meter opens the measurement window of the calibration system. This mode of operation is opposed to a calibrator that opens the measurement window at random time and that therefore may or may not catch certain pulses emitted by the meter.

Note: It is essential for a valid meter calibration to have the voltage stabilized a few seconds before the current is applied. This enables the Demo Code to initialize the 71M6531D/F and to stabilize the PLLs and filters in the CE. This method of operation is consistent with meter applications in the field as well as with metering standards.

Each meter phase must be calibrated individually. The procedures below show how to calibrate a meter phase with either three or five measurements. The PHADJ equations apply only when a current transformer is used for the phase in question. Note that positive load angles correspond to lagging current (see Figure 2-2).

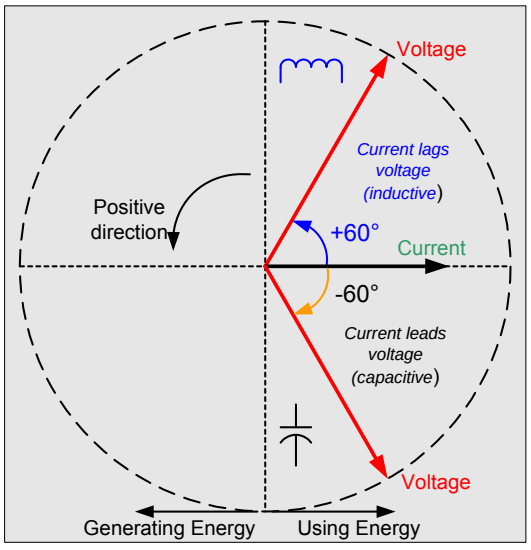


Figure 2-2: Phase Angle Definitions

The calibration procedures described below should be followed after interfacing the voltage and current sensors to the 71M6531D/F chip. When properly interfaced, the V3P3 power supply is connected to the meter neutral and is the DC reference for each input. Each voltage and current waveform, as seen by the 71M6531D/F, is scaled to be less than 250mV (peak).

2.2.2 CALIBRATION PROCEDURE WITH THREE MEASUREMENTS

The calibration procedure is as follows:

1. All calibration factors are reset to their default values, i.e. CAL_IA = CAL_VA = 16384, and PHADJ_A = 0.
2. An RMS voltage V_{ideal} consistent with the meter's nominal voltage is applied, and the RMS reading V_{actual} of the meter is recorded. The voltage reading error Axv is determined as

   $Axv = (V_{actual} - V_{ideal}) / V_{ideal}$
3. Apply the nominal load current at phase angles 0° and 60°, measure the Wh energy and record the errors E_0 AND E_{60}.
4. Calculate the new calibration factors CAL_IA, CAL_VA, and PHADJ_A, using the formulae presented in section 2.1.1 or using the spreadsheet presented in section 2.2.4.
5. Apply the new calibration factors CAL_IA, CAL_VA, and PHADJ_A to the meter. The memory locations for these factors are given in section 1.9.1.
6. Test the meter at nominal current and, if desired, at lower and higher currents and various phase angles to confirm the desired accuracy.
7. Store the new calibration factors CAL_IA, CAL_VA, and PHADJ_A in the EEPROM of the meter. If a Demo Board is calibrated, the methods shown in section 1.9.2 can be used.

2.2.3 CALIBRATION PROCEDURE WITH FIVE MEASUREMENTS

The calibration procedure is as follows:

1) All calibration factors are reset to their default values, i.e. CAL_IA = CAL_VA = 16384, and PHADJ_A = 0.
2) An RMS voltage V_{ideal} consistent with the meter's nominal voltage is applied, and the RMS reading V_{actual} of the meter is recorded. The voltage reading error Axv is determined as

   $Axv = (V_{actual} - V_{ideal}) / V_{ideal}$
3) Apply the nominal load current at phase angles 0°, 60°, 180° and –60° (-300°). Measure the Wh energy each time and record the errors E_0, E_{60}, E_{180}, and E_{300}.
4) Calculate the new calibration factors CAL_IA, CAL_VA, and PHADJ_A, using the formulae presented in section 2.1.2 or using the spreadsheet presented in section 2.2.4.
5) Apply the new calibration factors CAL_IA, CAL_VA, and PHADJ_A to the meter. The memory locations for these factors are given in section 1.9.1.
6) Test the meter at nominal current and, if desired, at lower and higher currents and various phase angles to confirm the desired accuracy.
7) Store the new calibration factors CAL_IA, CAL_VA, and PHADJ_A in the EEPROM of the meter. If the calibration is performed on a TERIDIAN Demo Board, the methods shown in sections 1.9.2 can be used.

2.2.4 PROCEDURE FOR AUTO-CALIBRATION

The fast calibration procedure is supported by the Demo Code when the Auto-Cal function is executed. This procedure requires the following steps:

1) Establish load voltage and current from the calibration system. The load angle must be exactly 0.00 degrees.
2) Enter the expected voltage and current using CLI commands. For example, to calibrate for 240V, 30A for two seconds, enter **`)F=2=+2400=+300.`**
3) Issue the CLI command **`CLB`**.
4) Wait the specified number of seconds.
5) Check the calibration factors established by the automatic procedure.

2.2.5 CALIBRATION SPREADSHEETS

Calibration spreadsheets are available from TERIDIAN Semiconductor. They are also included in the CD-ROM shipped with any Demo Kit. Figure 2-3 shows the spreadsheet for three measurements with three phases in use (only one phase needs to be used for the 71M6531D/F chip).

Figure 2-3 shows the spreadsheet for five measurements with three phases (only one phase needs to be used for the 71M6531D/F chip).

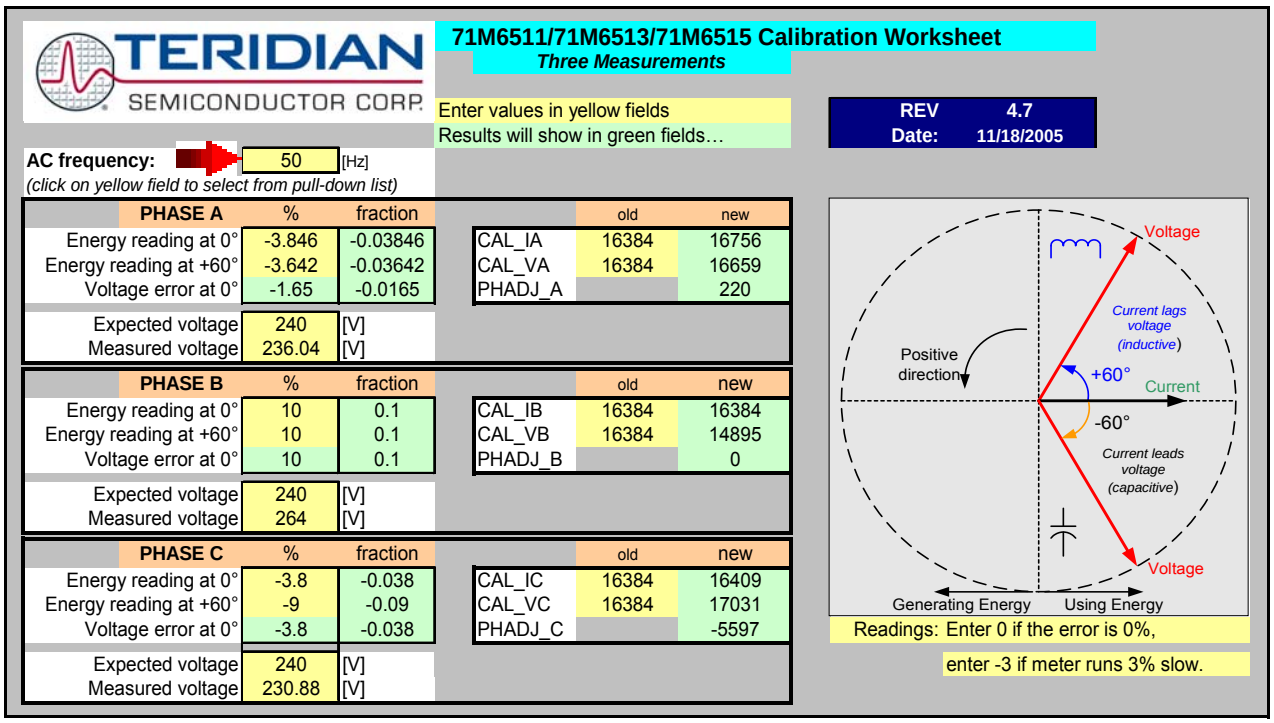
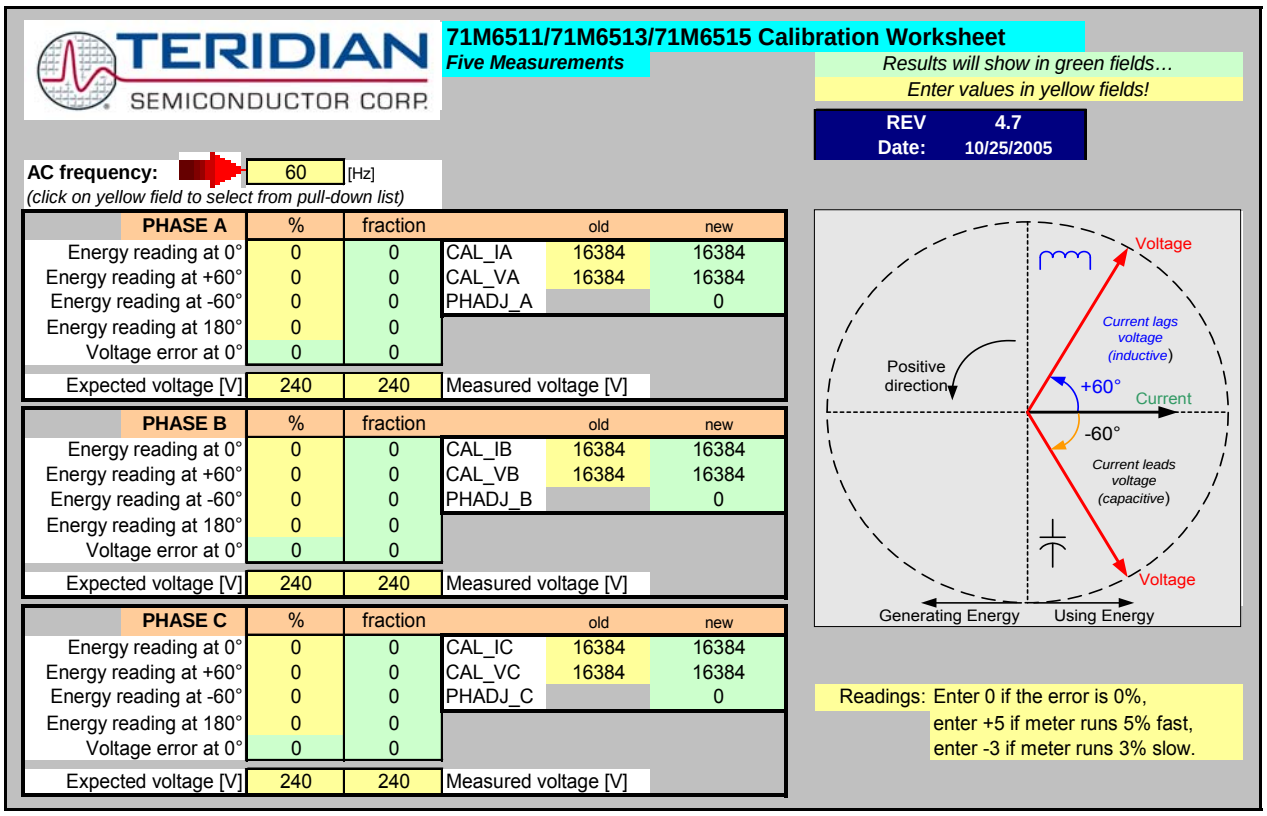


Figure 2-3: Calibration Spreadsheet for Three Measurements



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71M6511/71M6513/71M6515 Calibration Worksheet

Five Measurements

Results will show in green fields…
Enter values in yellow fields!

REV	4.7
Date:	10/25/2005

AC frequency: 60 [Hz]
(click on yellow field to select from pull-down list)

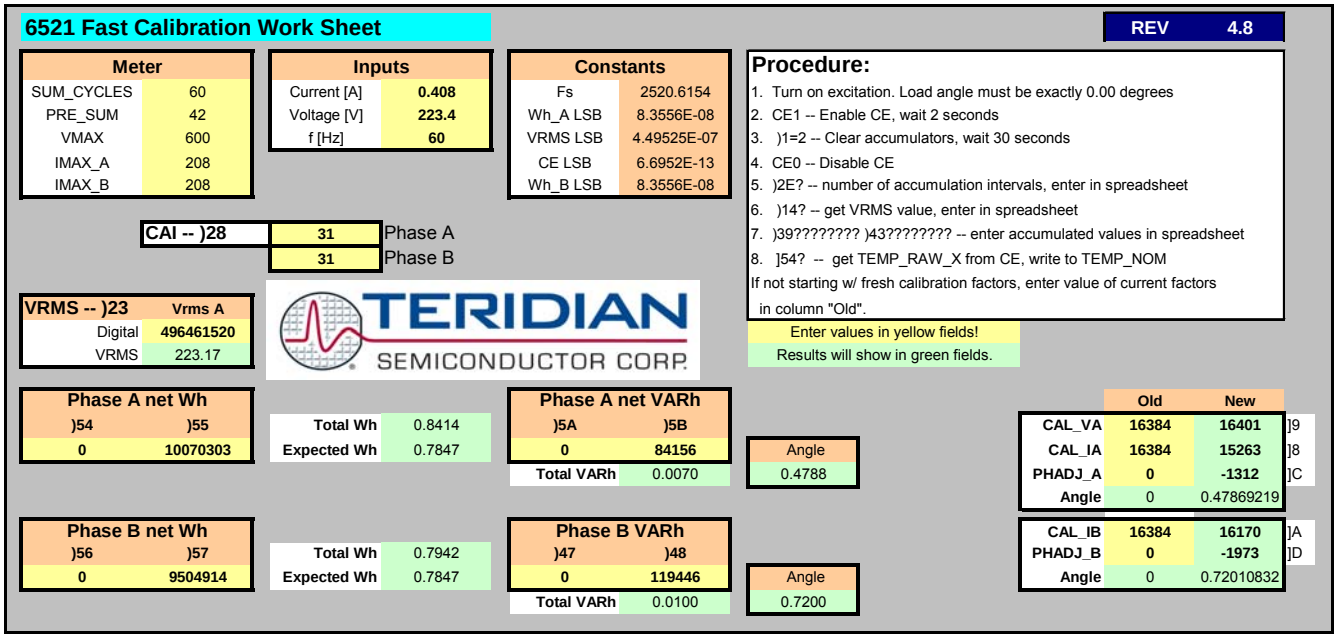
PHASE A	%	fraction		old	new
Energy reading at 0°	0	0	CAL_IA	16384	16384
Energy reading at +60°	0	0	CAL_VA	16384	16384
Energy reading at -60°	0	0	PHADJ_A		0
Energy reading at 180°	0	0			
Voltage error at 0°	0	0			
Expected voltage [V]	240	240	Measured voltage [V]		

PHASE B	%	fraction		old	new
Energy reading at 0°	0	0	CAL_IB	16384	16384
Energy reading at +60°	0	0	CAL_VB	16384	16384
Energy reading at -60°	0	0	PHADJ_B		0
Energy reading at 180°	0	0			
Voltage error at 0°	0	0			
Expected voltage [V]	240	240	Measured voltage [V]		

PHASE C	%	fraction		old	new
Energy reading at 0°	0	0	CAL_IC	16384	16384
Energy reading at +60°	0	0	CAL_VC	16384	16384
Energy reading at -60°	0	0	PHADJ_C		0
Energy reading at 180°	0	0			
Voltage error at 0°	0	0			
Expected voltage [V]	240	240	Measured voltage [V]		

Readings: Enter 0 if the error is 0%,
enter +5 if meter runs 5% fast,
enter -3 if meter runs 3% slow.

Figure 2-4: Calibration Spreadsheet for Five Measurements



6521 Fast Calibration Work Sheet

REV	4.8

Meter	
SUM_CYCLES	60
PRE_SUM	42
VMAX	600
IMAX_A	208
IMAX_B	208

Inputs	
Current [A]	0.408
Voltage [V]	223.4
f [Hz]	60

Constants	
Fs	2520.6154
Wh_A LSB	8.3556E-08
VRMS LSB	4.49525E-07
CE LSB	6.6952E-13
Wh_B LSB	8.3556E-08

Procedure:

1. Turn on excitation. Load angle must be exactly 0.00 degrees
2. CE1 -- Enable CE, wait 2 seconds
3.)1=2 -- Clear accumulators, wait 30 seconds
4. CE0 -- Disable CE
5.)2E? -- number of accumulation intervals, enter in spreadsheet
6.)14? -- get VRMS value, enter in spreadsheet
7.)39????????)43???????? -- enter accumulated values in spreadsheet
8.]54? -- get TEMP_RAW_X from CE, write to TEMP_NOM

If not starting w/ fresh calibration factors, enter value of current factors in column "Old".

CAI --)28	
31	Phase A
31	Phase B

VRMS --)23	Vrms A
Digital	496461520
VRMS	223.17

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Enter values in yellow fields!
Results will show in green fields.

Phase A net Wh	
)54	)55
0	10070303

Total Wh	0.8414
Expected Wh	0.7847

Phase A net VARh	
)5A	)5B
0	84156
Total VARh	0.0070

Angle
0.4788

Phase B net Wh	
)56	)57
0	9504914

Total Wh	0.7942
Expected Wh	0.7847

Phase B VARh	
)47	)48
0	119446
Total VARh	0.0100

Angle
0.7200

	Old	New	
CAL_VA	16384	16401	]9
CAL_IA	16384	15263	]8
PHADJ_A	0	-1312	]C
Angle	0	0.47869219	

CAL_IB	16384	16170	]A
PHADJ_B	0	-1973	]D
Angle	0	0.72010832	

Figure 2-5: Calibration Spreadsheet for Fast Calibration

2.2.6 COMPENSATING FOR NON-LINEARITIES

Nonlinearity is most noticeable at low currents, as shown in Figure 2-6, and can result from input noise and truncation. Nonlinearities can be eliminated using the *QUANT* variable.

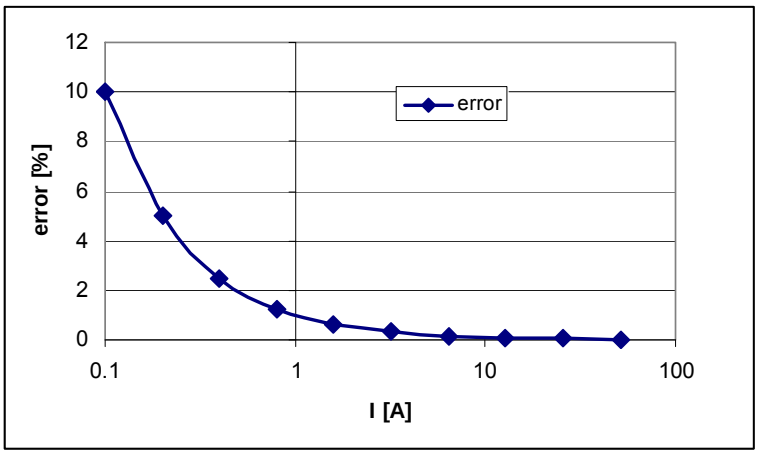

Figure 2-6: Non-Linearity Caused by Quantification Noise

The error can be seen as the presence of a virtual constant noise current. While 10mA hardly contribute any error at currents of 10A and above, the noise becomes dominant at small currents.

The value to be used for *QUANT* can be determined by the following formula:

$$QUANT = -\frac{\frac{error}{100} V \cdot I}{VMAX \cdot IMAX \cdot LSB}$$

Where error = observed error at a given voltage (V) and current (I),
VMAX = voltage scaling factor, as described in section 1.8.3,
IMAX = current scaling factor, as described in section 1.8.3,
LSB = *QUANT* LSB value = $7.4162*10^{-10}$W

Example: Assuming an observed error as in Figure 2-6, we determine the error at 1A to be +1%. If *VMAX* is 600V and *IMAX* = 208A, and if the measurement was taken at 240V, we determine *QUANT* as follows:

$$QUANT = -\frac{\frac{1}{100} 240 \cdot 1}{600 \cdot 208 \cdot 7.4162 \cdot 10^{-10}} = -11339$$

QUANT is to be written to the CE location 0x2F. It does not matter which current value is chosen as long as the corresponding error value is significant (5% error at 0.2A used in the above equation will produce the same result for *QUANT*).

Input noise and truncation can cause similar errors in the VAR calculation that can be eliminated using the *QUANT_VAR* variable. *QUANT_VAR* is determined using the same formula as *QUANT*.

2.2.7 CALIBRATING METERS WITH COMBINED CT AND SHUNT RESISTOR

In many cases it is desirable to discourage tampering by using two current sensors. The simple tampering method that involves connecting the low side of the load to earth ground (neutral) can be detected by adding a second current sensor in the neutral path, as shown in Figure 2-7.

In this configuration, the shunt resistor is connected to the IA channel while the current transformer is connected to the IB channel of the 71M6531D/F.

Calibrating this arrangement requires a few extra steps above the regular calibration. The calibration procedure applies to the sensor arrangement described above (SHUNT = IA, CT = IB).

Preparation:

1. Set the meter equation field of the configuration RAM for *EQU* to zero using the command: **RI00** = **10** (i.e. *EQU* = 0; *CE_EN* =1; *TMUX* = 0)
2. For the sake of calculation, individual *WRATE* parameters for Pulse generation, i.e. *WRATE_SHUNT* and *WRATE_CT* will be used.
3. It is also necessary to compute and estimate *IMAX_SHUNT* and *IMAX_CT* parameters for meter billing purposes.
4. Using *IMAX_SHUNT* and *VMAX*, the energy calculations for channel A should be performed.
5. The energy calculations for channel B should be performed using *IMAX_CT* and *VMAX*.
6. The LSB values for measurements for *W0SUM, W1SUM, VAR0SUM, VAR1SUM, I0SQSUM, I1SQSUM, V0SQSUM* should be modified to compute the correct energy values. That is, *IMAX_SHUNT* and *IMAX_CT* should be applied separately to individual channels based on the sensor connections.
7. Before starting a calibration, all calibration factors must be in their default state, i.e. *CAL_IA* (0x10), *CAL_VA* (0x11), *CAL_IB* (0x12) must be 16384. *PHADJ_A* (0x18) and *PHADJ_B* (0x19) should be zero.

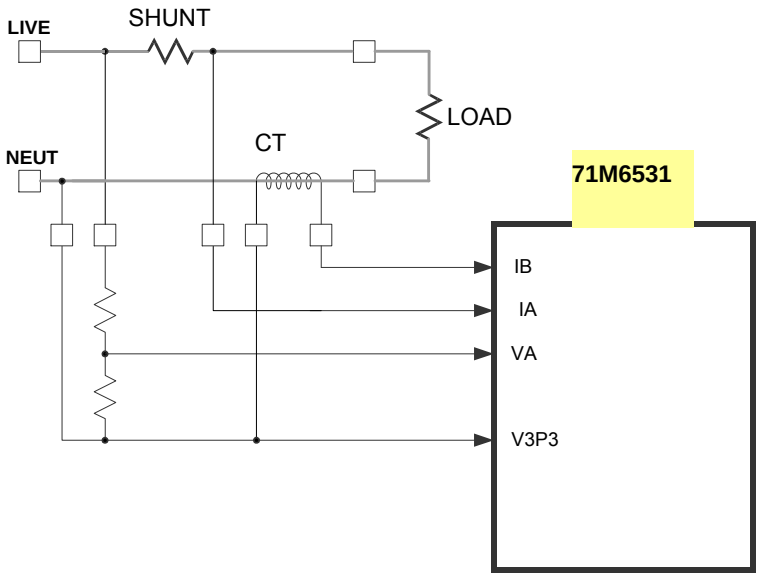

Figure 2-7: 71M6531 with Shunt and CT

Calibrating for Shunt Resistor (Channel A):

1. Calculate *IMAX* for the shunt resistor (*IMAX_SHUNT*). This can be done by using the following formula:

   IMAX_SHUNT = Vi_{MAX}/R_{SH}

   The Vi_{MAX} value is the maximum analog input voltage for the channel, typically 176.8mV (RMS), and R_{SH} is the resistance value of the shunt resistor.
   The value obtained for *IMAX_SHUNT* is stored at the MPU address 0x0A, using the command **)A=** *IMAX_SHUNT* of the Demo Code supplied by TERIDIAN.

2. Compute *WRATE_SHUNT* based on *IMAX_SHUNT* and *VMAX* and the formula given in 1.8.3:

   WRATE_SHUNT = (*IMAX_SHUNT* * *VMAX* * 47.1132) / (Kh * In_8 * N_{ACC} * X)

   Use *VMAX* = 600V (RMS) for the 6531 Demo Board if the resistor divider for VA has not been changed.

3. Update the *WRATE* register (at CE address 0x2D) with *WRATE_SHUNT*, using the command **]21=** *WRATE_SHUNT.*

4. Test for accuracy at 15A, 240V at phase angle 0, phase angle 60° and at phase angle –60°.

5. Apply the error values to the calibration spreadsheet (revision 2.0 or later) and determine the calibration factors for channel A, i.e. *CAL_IA*, *CAL_VA*, and *PHADJ_A*.

6. Update the CE registers 0x08, 0x09 and 0x0E of the compute engine with the calibration factors obtained from the spreadsheet, using the commands **]10=***CAL_IA*, **]11=***CALVA*, and **]18=***PHADJ_A*.

7. Retest for accuracy at several currents and phase angles.

At this point, channel A is calibrated. *WSUM* will be based on the voltage applied to the meter and the current flowing through the shunt resistor. The pulses generated will be based on the parameters entered for channel A.

Calibration for CT (Channel B):

1. Compute *IMAX* for the CT channel (*IMAX_CT*), based on the CT turns ratio N and the termination resistor value R_T using the formula:

   IMAX_CT = 176.8mV* N / R_T

   This value is used in the following step as *IMAX_CT*.

2. Compute *WRATE_CT* based on the values obtained for *IMAX_CT* and the formula given in 1.8.3:

   WRATE_CT = (*IMAX_CT* * *VMAX* * 47.1132) / (Kh * *In_8* * N_{ACC} * X)

3. Update the *WRATE* register (CE address 0x2D) with *WRATE_CT*, using the command **]21=** *WRATE_CT.*

4. Enter the command **>)7=2.** Configure *W1SUM* as external pulse source since the CT is connected to channel 1 for VA*IB.

5. Test for accuracy at 15A, 240V at phase angle 0, phase angle 60° and at phase angle –60°.

6. Apply these values to the calibration spread sheet (revision 2.0 or later) and derive the calibration factor *PHADJ_B*.

7. Update only the CE address 0x0F with the value for *PHADJ_B* using the command **]19=** *PHADJ_B.*

8. Adjust *CAL_IB* for the total error found in the accuracy test using the formula

   CAL_IB = 16384 * (1 - error/100)

That is, if the chip reports an error of -2.5%, *CAL_IB* should be adjusted to a value of

(16384 * (1 - (-2.5/100)).

9. Since *CAL_VA* and *CAL_IA* have already been adjusted for channel A, these registers should not be updated.
10. Retest for accuracy at several currents and phase angles.

After completing the calibration, the energy values W0SUM, based on VA*IA and *W1SUM*, based on VA*IB are accessible to the MPU firmware. The pulse rate is controlled by *W1SUM* and determined by the parameters selected for the CT channel (VA, IB). Differences between *W0SUM* and *W1SUM*, indicating tampering, can be detected by the MPU for each accumulation interval.

Note: The user has to customize the Demo Code to utilize the values obtained from the VA, IA, and IB channels for proper calculation of tariffs.

Table 2-1 summarizes the important parameters used in the calibration procedure.

Channel	Sensor	Formula	Parameters	W Pulse Generation	VAR Pulse Generation
A	Shunt Resistor	*WASUM* = VA*IA *VARASUM* = VA*IA	*VMAX* = *VMAX* *IMAX* = IMAX_SHUNT *WRATE* = WRATE_SHUNT	*WASUM*	*VARASUM*
B	CT	*WBSUM* = VA*IB *VARBSUM* = VA*IB	*VMAX* = *VMAX* *IMAX* = IMAX_CT *WRATE* = WRATE_CT	*WBSUM*	*VARBSUM*

Table 2-1: Calibration Summary

2.3 CALIBRATING AND COMPENSATING THE RTC

The real-time clock (RTC) of the 71M6534 is controlled by the crystal oscillator and thus only as accurate as the oscillator. The 71M6534 has two rate adjustment mechanisms:

- Analog rate adjustment, using the I/O RAM register *RTCA_ADJ[6:0]*. This adjustment is used to set the oscillator frequency at room temperature close to the target (ideal) value. Adjusting *RTCA_ADJ[6:0]* will change the time base used for energy measurements and thus slightly influence these energy measurements. Therefore it is recommended to adjust the RTC before calibrating a meter.
- Digital rate adjustment is used to dynamically correct the oscillator rate under MPU control. This is necessary when the IC is at temperatures other than room temperature to correct for frequency deviations.

The analog rate adjustment uses the I/O RAM register *RTCA_ADJ[6:0]*, which trims the crystal load capacitance. Setting *RTCA_ADJ[6:0]* to 00 minimizes the load capacitance, maximizing the oscillator frequency. Setting *RTCA_ADJ[6:0]* to 3F maximizes the load capacitance, minimizing the oscillator frequency.

The maximum adjustment is approximately ±60ppm. The precise amount of adjustment will depend on the crystal and on the PCB properties. The adjustment may occur at any time, and the resulting clock frequency can be measured over a one-second interval using a frequency counter connected to the TMUXOUT pin, while 0x10 or 0x11 is selected for the I/O RAM register *TMUX*[4:0]. Selecting 0x10 will generate a 1-second output; selecting 0x11 will generate a 4-second output. The 4-second output is useful to adjust the oscillator at high accuracy. It is also possible to set *TMUX*[4:0] to 0x1D to generate a 32.768kHz output.

The adjustment of the oscillator frequency using *RTCA_ADJ[6:0]* at room temperature will cause the 71M6534 IC to maintain the adjusted frequency

The digital rate adjustment can be used to adjust the clock rate up to ±988ppm, with a resolution of 3.8ppm. The clock rate is adjusted by writing the appropriate values to *PREG[16:0]* and *QREG[1:0]*. The default frequency is 32,768 RTCLK cycles per second. To shift the clock frequency by Δ ppm, calculate *PREG* and *QREG* using the following equation:

$$4 \cdot PREG + QREG = floor\left(\frac{32768 \cdot 8}{1 + \Delta \cdot 10^{-6}} + 0.5\right)$$

PREG and *QREG* form a single adjustment register with *QREG* providing the two LSBs. The default values of *PREG* and *QREG*, corresponding to zero adjustment, are 0x10000 and 0x0, respectively. Setting both *PREG* and *QREG* to zero is illegal and disturbs the function of the RTC.

If the crystal temperature coefficient is known, the MPU can integrate temperature and correct the RTC time as necessary, using *PREG[16:0]* and *QREG[1:0]*.

The Demo Code adjusts the oscillator clock frequency using the parameters *Y_CAL*, *Y_CAL1* and *Y_CAL2,* which can be obtained by characterizing the crystal over temperature. Provided the IC substrate temperature tracks the crystal temperature, the Demo Code adjusts the oscillator within very narrow limits.

The MPU Demo Code supplied with the TERIDIAN Demo Kits has a direct interface for these coefficients and it directly controls the *PREG[16:0]* and *QREG[1:0]* registers. The Demo Code uses the coefficients in the following form:

$$CORRECTION(ppm) = \frac{Y\_CAL}{10} + T \cdot \frac{Y\_CALC}{100} + T^2 \cdot \frac{Y\_CALC2}{1000}$$

Note that the coefficients are scaled by 10, 100, and 1000 to provide more resolution.

Example: For a crystal, the deviations from nominal frequency are curve fitted to yield the coefficients a = 10.89, b = 0.122, and c = –0.00714. The coefficients for the Demo Code then become (after rounding, since the Demo Code accepts only integers):

Y_CAL = -109, *Y_CALC* = 12, *Y_CALC2* = 7

2.4 TESTING THE DEMO BOARD

This section will explain how the 71M6531D/F IC and the peripherals can be tested. Hints given in this section will help evaluating the features of the Demo Board and understanding the IC and its peripherals.

2.4.1 FUNCTIONAL METER TEST

This is the test that every Demo Board has to pass before being integrated into a Demo Kit. Before going into the functional meter test, the Demo Board has already passed a series of bench-top tests, but the functional meter test is the first test that applies realistic high voltages (and current signals from current transformers) to the Demo Board.

Figure 2-8 shows a meter connected to a typical calibration system. The calibrator supplies calibrated voltage and current signals to the meter. It should be noted that the current flows through the CT or CTs that are not part of the Demo Board. The Demo Board rather receives the voltage output signals from the CT. An optical pickup senses the pulses emitted by the meter and reports them to the calibrator (some calibration systems have electrical pickups). The calibrator measures the time between the pulses and compares it to the expected time, based on the meter Kh and the applied power.

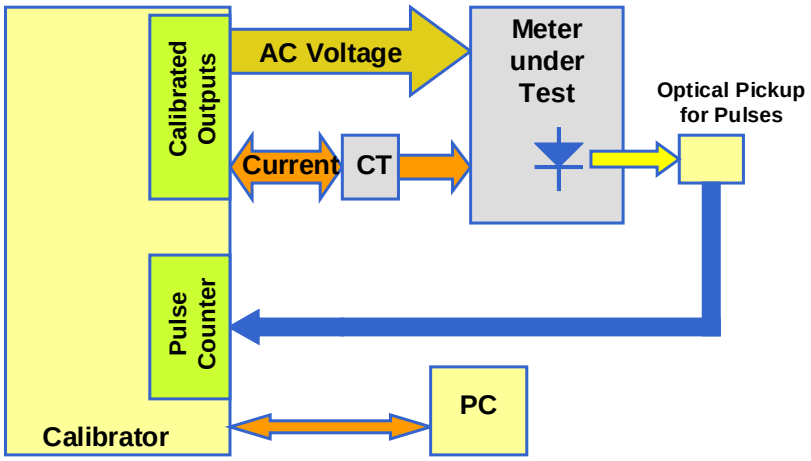

Figure 2-8: Meter with Calibration System

TERIDIAN Demo Boards are not calibrated prior to shipping. However, the Demo Board pulse outputs are tested and compared to the expected pulse output. Figure 2-9 shows the screen on the controlling PC for a typical Demo Board. The number in the red field under "As Found" represents the error measured for phase A, while the number in the red field under "As Left" represents the error measured for phase B. Both numbers are given in percent. This means that for the measured Demo Board, the sum of all errors resulting from tolerances of PCB components, CTs, and 71M6531D/F tolerances was –2.8% and –3.8%, a range that can easily be compensated by calibration.

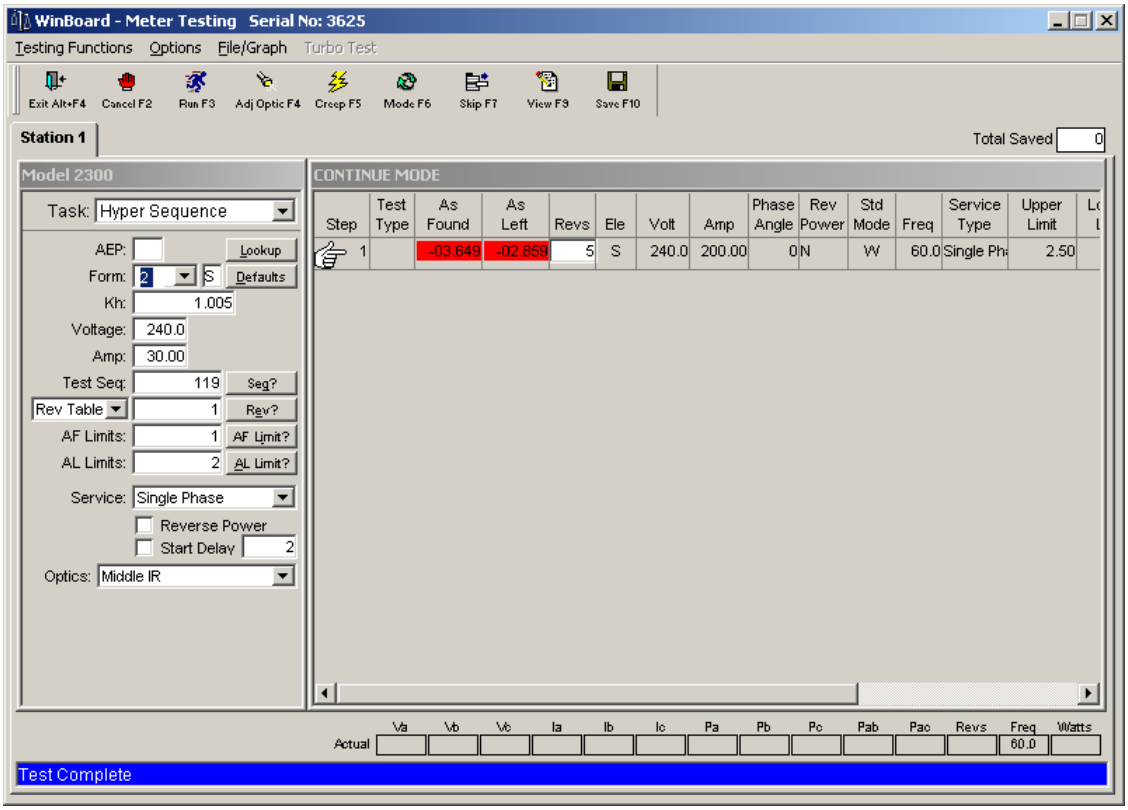

Figure 2-9: Calibration System Screen

2.4.2 EEPROM

Testing the EEPROM provided on the Demo Board is straightforward and can be done using the serial command line interface (CLI) of the Demo Code.

To write a string of text characters to the EEPROM and read it back, we apply the following sequence of CLI commands:

>EEC1 Enables the EEPROM

>EESthis is a test Writes text to the buffer

>EET80 Writes buffer to address 80

Written to EEPROM address 00000080 74 68 69 73 20 69 73 20 61 ….

Response from Demo Code

>EER80.E Reads text from the buffer

Read from EEPROM address 00000080 74 68 69 73 20 69 73 20 61 ….

Response from Demo Code

>EEC0 Disables the EEPROM

2.4.3 RTC

Testing the RTC inside the 71M6531D/F IC is straightforward and can be done using the serial command line interface (CLI) of the Demo Code.

To set the RTC and check the time and date, we apply the following sequence of CLI commands:

>M10 LCD display to show calendar date

>RTD05.09.27.3 Sets the date to 9/27/2005 (Tuesday)

>M9 LCD display to show time of day

>RTT10.45.00 Sets the time to 10:45:00. AM/PM distinction: 1:22:33PM = 13:22:33

2.4.4 HARDWARE WATCHDOG TIMER

The hardware WDT of the 71M6534/6534H is disabled when the voltage at the V1 pin is at 3.3V (V3P3). On the Demo Boards, this is done by plugging in a jumper at TP10 between the V1 and V3P3 pins.

Conversely, removing the jumper at TP10 will enable the WDT. When the WDT is enabled, typing "W" at the command line interface will cause the Demo Board to reset.

2.4.5 LCD

Various tests of the LCD interface can be performed with the Demo Board, using the serial command line interface (CLI):

The display outputs are enabled by setting the *LCD_EN* register to 1.

Register Name	Address [bits]	R/W	Description
LCD_EN	2021[5]	R/W	Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 are ground as are the COM and SEG outputs.

To access the *LCD_EN* register, we apply the following CLI commands:

>RI21$ Reads the hex value of register 0x2021

>25 Response from Demo Code indicating the bit 5 is set

>RI21=5 Writes the hex value 0x05 to register 0x2021 causing the display to be switched off

>RI21=25 Sets the *LCD_EN* register back to normal

The *LCD_CLK* register determines the frequency at which the COM pins change states. A slower clock means lower power consumption, but if the clock is too slow, visible flicker can occur. The default clock frequency for the 71M6531 Demo Boards is 150Hz (*LCD_CLK* = 01).

Register Name	Address [bits]	R/W	Description
LCD_CLK[1:0]	2021[1:0]	R/W	Sets the LCD clock frequency, i.e. the frequency at which SEG and COM pins change states. Note: f_w = CKADC/128 = 38,400 00: $f_w/2^9$, 01: $f_w/2^8$, 10: $f_w/2^7$, 11: $f_w/2^6$

To change the LCD clock frequency, we apply the following CLI commands:

>**RI21$** Reads the hex value of register 0x2021

>**25** Response from Demo Code indicating the bit 0 is set and bit 1 is cleared.

>**RI21=24** Writes the hex value 0x24 to register 0x2021 clearing bit 0 – LCD flicker is visible now

>**RI21=25** Writes the original value back to *LCD_CLK*

2.4.6 SUPPLY CURRENT MEASUREMENTS

Some precautions have to be taken when exact supply current measurements are to be made. Supplying unnecessary pull-up resistors and/or external components with current will yield inaccurate measurement results. In brownout mode, the following precautions should be taken:

1) The Debug Board should be removed from the Demo Board.
2) The RX pin should be properly terminated, e.g. by tying it to GND. On the Demo Boards, this is accomplished with R90.
3) The jumper on JP4 should be moved to position 1-2 in order to save the current required to supply the ICE_E pin.

2.5 TERIDIAN APPLICATION NOTES

Please contact your local TERIDIAN sales representative for TERIDIAN Application Notes.

3

3 HARDWARE DESCRIPTION

3.1 DEMO BOARD DESCRIPTION: JUMPERS, SWITCHES, TEST POINTS AND CONNECTORS

This description covers the D6531N12A2 Demo Board.

The items described in the following tables refer to the flags in Figure 3-1.

Item # (Figure 3.1)	Schematic & Silk Screen Reference	Name	Use
1	J4	VA_IN 	This is the line voltage input that feeds both the resistor divider leading to the VA pin on the chip and the internal power supply. The line voltage wire is connected to the spade terminal on the bottom of the board.. **Caution: High Voltage. Do not touch this pin!**
2	TP3	--	1-pin header allowing access to the V3P3 voltage generated by the board power supply.
3	JP1	PS_SEL	Power source selector. If a jumper is installed, the Demo Board is powered by the line voltage on phase A.
4	TP15	GND	Test point for board ground
5	TP2	VA, REFA	2-pin header test point. Pin 1 is the VA line voltage input to the IC, pin 2 is V3P3.
6	JP14	YPULSE	2-pin header used as a selector for the driving source of pulse LED D6. In **default setting (2-3), the WPULSE** (DIO6) drives the LED. The alternative selection causes the XPULSE output to drive the LED. Starting with **Demo Code revision 4p6**, the CE will activate the YPULSE when a sag condition is encountered. Placing a jumper across pins 2 and 3 will activate the VARh LED when a sag condition is detected which can help with sag threshold testing.
7	JP13	XPULSE	2-pin header used as a selector for the driving source of LED D5. In **default setting (1-2), the VARPULSE** (DIO7) drives the LED. The alternative selection causes the YPULSE output to drive the LED.

Table 3-1: 71M6531 Demo Board description: 1/3

Item # (Figure 3.1)	Schematic & Silk Screen Reference	Name	Use
8	JP12	BAT_MODE	This 3-pin header allows selection of the battery mode operation: A jumper across pins 1-2 indicates that **no external battery** is available. The 71M6531D/F will stay in brownout mode when system power is down and it will communicate at 9600bd. A jumper across pins 2-3 indicates that an **external battery** is available. The 71M6531D/F will be able to transition from brownout mode to sleep and LCD modes when system power is down and it will communicate at 300bd.
9	J12	V3P3, OTX, V3P3, ORX, GND	5-pin header. Pins 1 and 3 carry the supply voltage to the 6531D/F IC. Pin 2 is the TX_OPT output of the 6531D/F IC. Pin 4 is the OPT_RX input to the 6531D/F IC. Pin 5 is ground.
10	D6	VARh	VARh LED
11	TP22	VARh	Test points for pulses generated by the VARh LED.
12	TP21	Wh	Test points for pulses generated by the Wh LED.
13	D5	Wh	Wh LED.
14	JP8	GND, VBAT	3-pin header for connection of an external battery (+ at pin 2, - at pin 3). If no battery is connected, a jumper must be installed across pins 1-2.
15	SW1	RESET	Chip reset switch: The RESET pin has an internal pull-down that allows normal chip operation. When the switch is pressed, the RESET pin is pulled high which resets the IC into a known state. **Note: The RESET button is disabled in the Demo Board default configuration. The RESET button can be enabled by removing R91.**
16	JP4	ICE enable	Selector for ICE/regular operation: **Jumper 1-2 = regular operation (default)** Jumper 2-3 = ICE operation **Remove this jumper for brownout current measurements!**
17	U5	--	The 71M6531D/F IC (QFN-68)
18	U7	--	LCD
19	TP17	TMUXOUT	2-pin header providing test points for TMUXOUT and CKTEST.
20	J17	SPI Interface	This 2x5 header provides access to the SPI interface.
21	J2	DEBUG	Connector for plugging in the Debug Board, either directly or via a flat ribbon cable.
22	J15	--	An emulator or flash programmer can be connected to this 6-pin header. For production units, this would be a more economical alternative to J14.
23	SW2	PB	Pushbutton used to wake up the chip when in sleep or LCD mode. This button can also be used in Mission Mode to cycle the display.
24	J14	EMULATOR I/F	2x10 male header with 0.05" pitch on the back side of the board. The connector of the Signum ADM51 emulator or TFP-2 programmer can be plugged into J14. Alternatively, J15 can be used.
25	TP10	V1, V3P3	2-pin header representing the V1 comparator voltage input test point and ground. A jumper should be placed between V1 and V3P3 to disable the watchdog timer.

Table 3-2: 71M6531 Demo Board description: 2/3

Item # (Figure 3.1)	Schematic & Silk Screen Reference	Name	Use
26	TP1	IA, V3P3	2-pin header test point. Pin 1 is the IA input to the IC and pin 2 is V3P3.
27	TP19	IB, V3P3	2-pin test point. Pin 1 is the IB input to the IC and pin 2 is the V3P3 reference.
28	J3	IA_IN	3-pin header on the bottom of the board for connection of the CT for phase A. Pin 3 may be used to ground an optional cable shield. In shunt configuration, two wires from the shunt resistor representing the voltage across the shunt are connected to pins 1 and 2.
29	J16	IB_IN	3-pin header on the bottom of the board for connection of the CT for phase B. Pin 3 may be used to ground an optional cable shield.
30	TP4	VB, REFB	2-pin header test point. Pin 1 is the VB line voltage input to the IC, pin 2 is V3P3.
31	J5	VB_IN 	This is the line voltage input that feeds both the resistor divider leading to the VB pin on the chip. The line voltage wire is connected to the spade terminal on the bottom of the board. **Caution: High Voltage. Do not touch this pin!**
32	J1	5VDC	Plug for connection of the external 5 VDC power supply.
33	J9	NEUTRAL	This is the NEUTRAL line voltage input. It is connected to the 3.3V net of the 71M6531D/F. The neutral wire is connected to the spade terminal on the bottom of the board.

Table 3-3: 71M6531 Demo Board description: 3/3

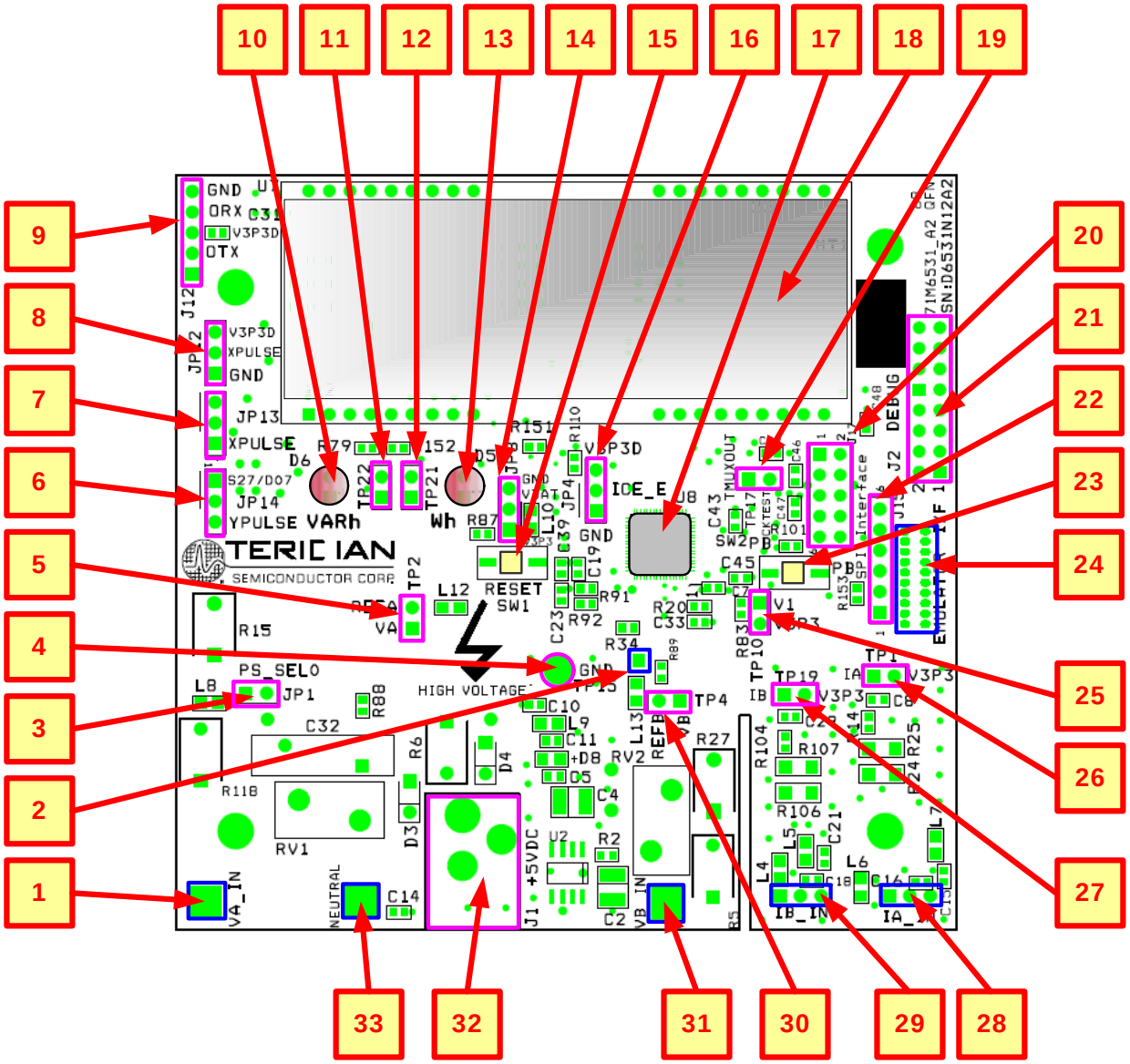

Figure 3-1: 71M6531N12A2 Board Connectors, Jumpers, Switches, and Test Points

3.2 DEMO BOARD HARDWARE SPECIFICATIONS

PCB Dimensions

Dimensions	3.625" x 3.625" (92.075mm x 92.075mm)
Thickness	0.062" (1.6mm)
Height w/ components	2.0" (51mm)

Environmental

Operating Temperature (accuracy of crystal oscillator affected outside –10°C to +60°C)	-40°…+85°C
Storage Temperature	-40°C…+100°C

Power Supply

Using AC Input Signal	180V…700V rms
DC Input Voltage (powered from DC supply)	5VDC ±0.5V
Supply Current	25mA typical

Input Signal Range

AC Voltage Signal (VA)	0…240V rms
AC Current Signals (IA, IB) from sensor	0…0.25V p/p

Interface Connectors

DC Supply Jack (J1) to Wall Transformer	Concentric connector, 2.5mm
Emulator (J14)	10x2 Header, 0.05" pitch
Emulator (J15)	5x1 Header, 0.1" pitch
SPI	5x2 header, 0.1" pitch
Input Signals	Spade terminals and 0.1" headers on PCB bottom
Debug Board (J2)	8x2 Header, 0.1" pitch
Target Chip (U8)	QFN68

Functional Specification

Time Base Frequency	32.768kHz, ±20PPM at 25°C

Controls and Displays

Reset	Button (SW2)
Numeric Display	8-digit LCD, 14-segments, 7mm character height
"Watts", "VARS"	red LEDs (D5, D6)

Measurement Range

Voltage	120…700 V rms (resistor division ratio 1:3,398)
Current	CT: 1.7Ω termination for 2,000:1 CT (IMAX=208A), Shunt: Depending on shunt resistance R_S IMAX = 176mV/R_S

Regulatory Compliance

RoHS	PCB, components, and processing are in compliance with the RoHS guidelines.

4

4 APPENDIX

This appendix includes the following documentation, tables and drawings:

Demo Board Schematics

Demo Board Bills of Materials (Parts Lists - BOM)

Demo Board PCB Layout Views

Debug Board Description

Debug Board Electrical Schematic
Debug Board Bill of Materials
Debug Board PCB Layout

71M6531D/F Pin-Out and Mechanical Description

71M6531D/F Pin Description
71M6531D/F Pin-out

Modification History

4.1 71M6531N12A2 DEMO BOARD ELECTRICAL SCHEMATIC

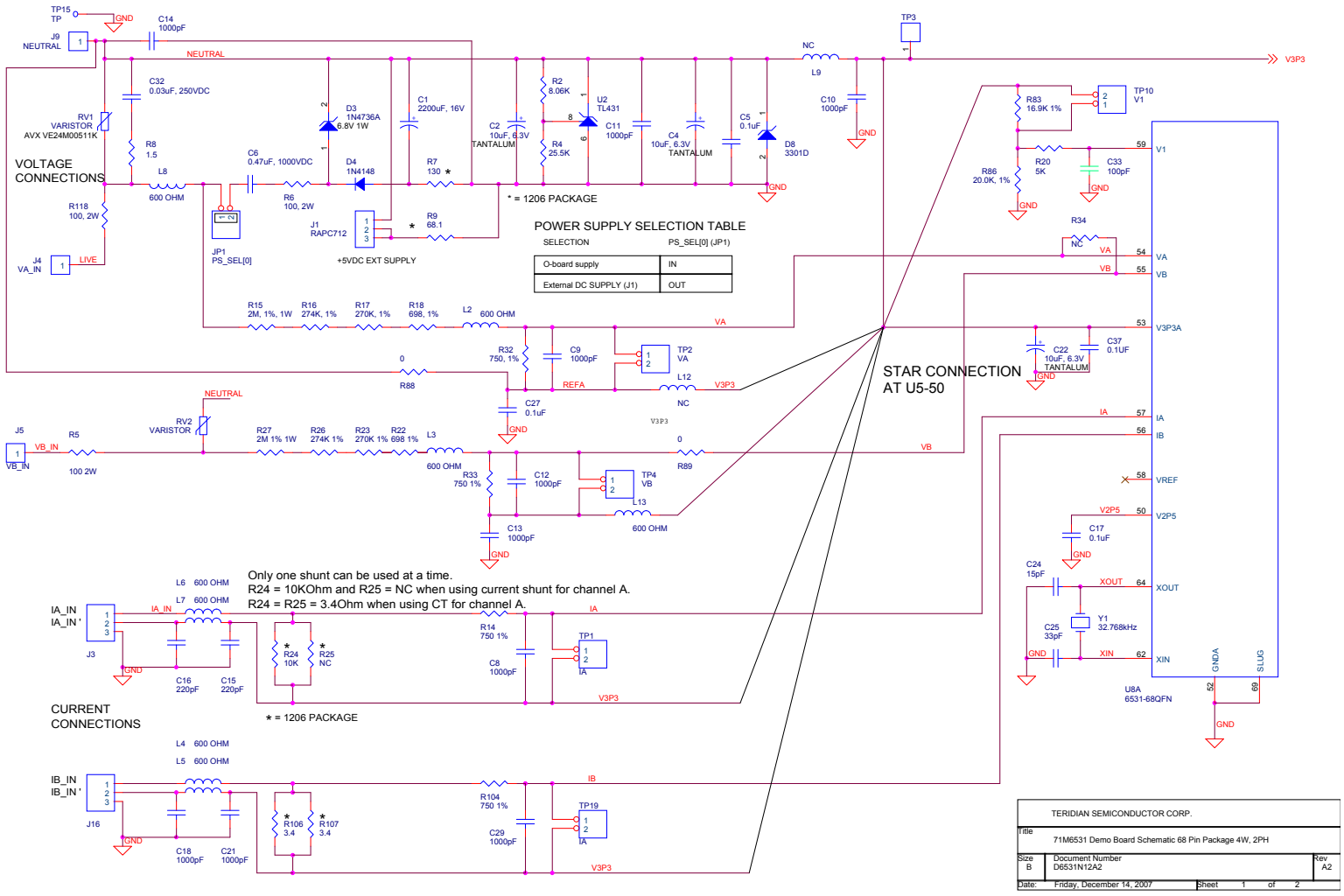

Figure 4-1: 71M6531N12A2 Demo Board (REV 2.0): Electrical Schematic 1/3 – Shunt Configuration

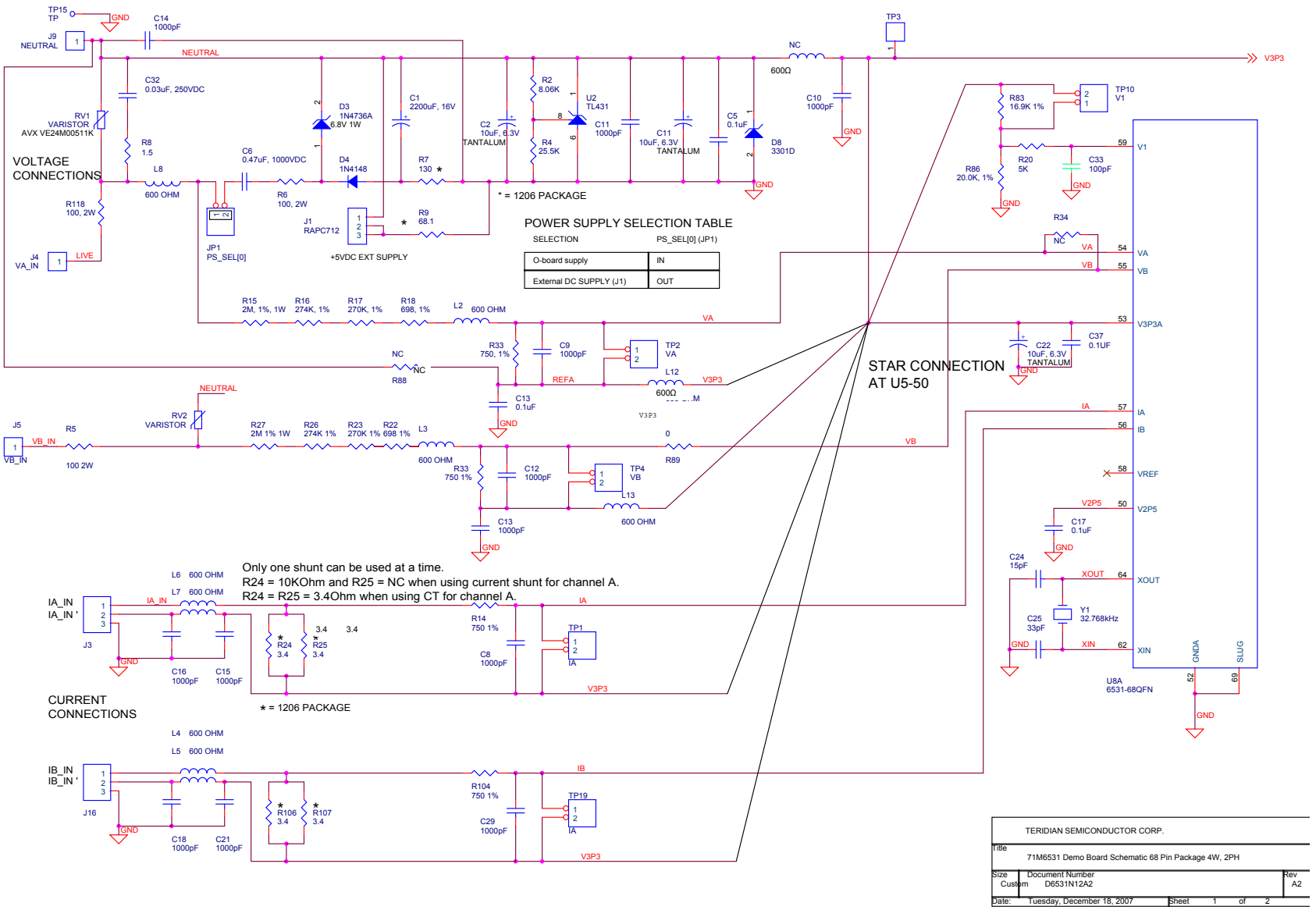

Figure 4-2: 71M6531N12A2 Demo Board (REV 2.0): Electrical Schematic 2/3 – CT Configuration

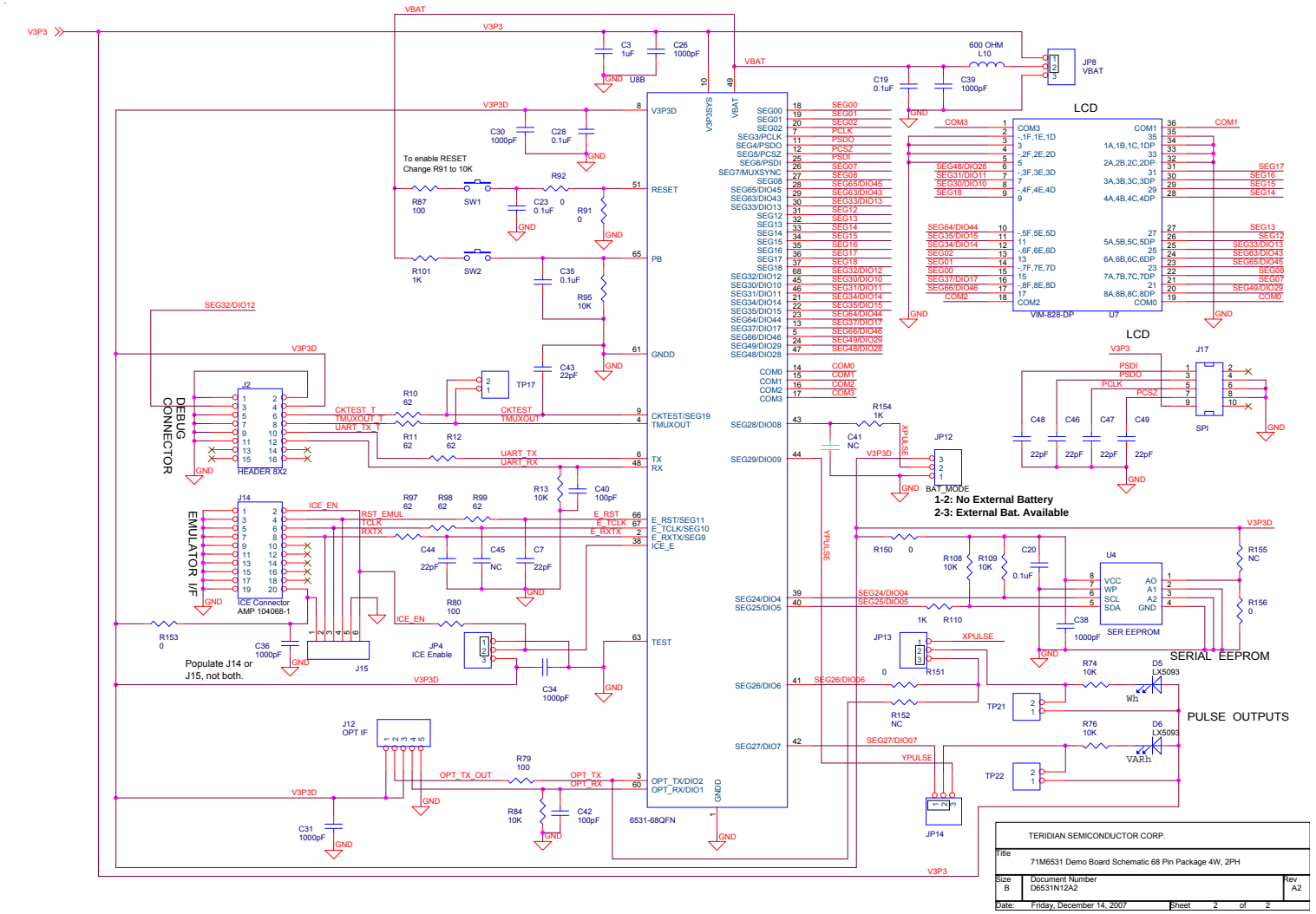

Figure 4-3: 71M6531N12A2 Demo Board (REV 2.0): Electrical Schematic 3/3 – Digital Section

4.2 71M6531N12A2 DEMO BOARD BILL OF MATERIAL

Item	Q	Reference	Part	PCB Footprint	Digi-Key/Mouser Part Number	Part Number	Manufacturer
1	1	C1	2200uF	radial	P5143-ND	ECA-1CM222	Panasonic
2	3	C2,C4,C22	10uF	RC1812	478-1672-1-ND	TAJB106K010R	AVX
3	1	C3	1uF	RC0603	PCC2224CT-ND	ECJ-1VB1C105K	Panasonic
4	9	C5,C17,C19,C20,C23,C27,C28,	0.1uF	RC0603	445-1314-1-ND	C1608X7R1H104K	TDK
		C35,C37					
5	1	C6	0.47uF		BC1918-ND	2222 383 30474	BC Components
6	7	C7,C43,C44,C46-C49	22pF	RC0603	445-1273-1-ND	C1608C0G1H220J	TDK
7	15	C8-C14,C26,C29-C31, C34,C36,C38,C39	1000pF	RC0603	445-1298-1-ND	C1608X7R2A102K	TDK
8	1	C24	15pF	RC0603			
9	1	C25	33pF	RC0603	445-1275-1-ND	C1608C0G1H330J	TDK
10	2	C41,C45	NC	RC0603	445-2171-1-ND	C1608COH1H150J	TDK
11	1	C32	0.03uF	axial	75-125LS30-R	125LS30-R	Vishay
12	5	C18,C21,C33,C40,C42	100pF	RC0603	445-1281-1-ND	C1608C0G1H101J	TDK
13	2	C15,C16	220pF	RC0603	445-1285-1-ND	C1608COG1H221J	TDK
14	1	D3	6.8V ZENER	D041	1N4736ADICT-ND	1N4736A-T	DIODES
15	1	D4	Switching Diode	D035	1N4148DICT-ND	1N4148-T	DIODES
16	2	D5,D6	LED	radial	404-1104-ND	H-3000L	Stanley
17	1	D8	UCLAMP3301D	SOD-323	--	UCLAMP3301D.TCT	SEMTECH
18	1	J1	DC CONNECTOR		SC237-ND	RAPC712X	Switchcraft
19	1	J2	HEADER 8X2	8X2PIN	S2011E-36-ND	PZC36DAAN	Sullins
20	2	J3,J16	HEADER 3	3X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
21	3	J4,J5,J9	Spade Terminal		A24747CT-ND	62395-1	AMP
22	1	J12	HEADER 5	5X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
23	1	J14	10X2 CONNECTOR, 0.05"		571-5-104068-1	5-104068-1	AMP
24	1	J15	HEADER 6	6X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
25	1	J17	HEADER 5X2	5X2PIN	S2011E-36-ND	PZC36DAAN	Sullins
26	1	JP1	HEADER 2	2X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
27	5	JP4,JP8,JP12,JP13,JP14	HEADER 3	3X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
28	11	L2-L10,L12,L13	Ferrite bead, 600 Ohm	RC0805	445-1556-1-ND	MMZ2012S601A	TDK
29	2	RV1,RV2	VARISTOR	radial	594-2381-594-55116	238159455116	Vishay
30	1	R2	8.06K, 1%	RC0603	P8.06KHCT-ND	ERJ-3EKF8061V	Panasonic
31	1	R4	25.5K, 1%	RC0603	P25.5KHCT-ND	ERJ-3EKF2552V	Panasonic
32	3	R5,R6,R118	100, 2W	axial	100W-2-ND	RSF200JB-100R	Yageo
33	1	R7	130, 1%	RC1206	P130FCT-ND	ERJ-8ENF1300V	Panasonic
34	1	R8	1.5	RC1206	P1.5ECT-ND	ERJ-8GEYJ1R5V	Panasonic
35	1	R9	68.1	RC1206	P68.1FCT-ND	ERJ-8ENF68R1V	Panasonic
36	6	R10,R11,R12,R97,R98,R99	62	RC0603	P62GCT-ND	ERJ-3GEYJ620V	Panasonic
37	8	R13,R24,R74,R76,	10K	RC0603	P10KGCT-ND	ERJ-3GEYJ103V	Panasonic
		R84,R95,R108,R109					
38	4	R14,R32,R33,R104	750, 1%	RC0603	P750HCT-ND	ERJ-3EKF7500V	Panasonic
39	2	R15,R27	2M, 1%	axial	71-RN65DF-2.0M	RN65D2004FB14	Dale
40	2	R16,R26	274K, 1%	RC0805	P274KCCT-ND	ERJ-6ENF2743V	Panasonic
41	2	R17,R23	270K, 1%	RC0805	RHM270KCCT-ND	MCR10EZHF2703	Rohm
42	2	R18,R22	698, 1%	RC0805	P698CCT-ND	ERJ-6ENF6980V	Panasonic
43	1	R20	4.99K, 1%	RC0603	P4.99KHCT-ND	ERJ-3EKF4991V	Panasonic
44	3	R79,R80,R87	100	RC0603	P100HCT-ND	ERJ-3EKF1000V	Panasonic
45	2	R106,R107	3.4, 1%	RC1206	311-3.40FRCT-ND	RC1206FR-073R40L	Yageo
46	4	R25,R34,R152,R155	NC	RC0603			
47	1	R83	16.9K, 1%	RC0603	P16.9KHCT-ND	ERJ-3EKF1692V	Panasonic
48	1	R86	20K, 1%	RC0603	P20.0KHCT-ND	ERJ-3EKF2002V	Panasonic
49	3	R101,R110,R154	1K	RC0603	P1.0KGCT-ND	ERJ-3GEYJ102V	Panasonic
50	8	R88,R89,R91,R92,R150,R151,	0	RC0603	P0.0GCT-ND	ERJ-3GEY0R00V	Panasonic
		R153,R156					
51	2	SW1,SW2			P8051SCT-ND	EVQ-PJX05M	Panasonic
52	8	TP1,TP2,TP4,TP10,TP17,TP19,	HEADER 2	2X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
53		TP21,TP22					
54	1	TP3	HEADER 1	1X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
55	1	TP15	Test Point		5011K-ND	5011	Keystone
56	1	U2	REGULATOR, 1%	SO8	296-1288-1-ND	TL431AIDR	Texas Instruments
57	1	U4	SER EEPROM	SO8	AT24C256BN-10SU-1.8-ND	AT24C256BN-10SU-1.8	ATMEL
58	1	U8	71M6531	68QFN	--	71M6531-IM	TERIDIAN
59	1	U7	VIM-828-DP	LCD VIM-828	153-1110-ND	VIM-828-DP13.2-RC-S-LV	VARITRONIX
60	1	Y1	32.768kHz		XC1195CT-ND	ECS-.327-12.5-17X-TR	ECS

Table 4-1: 71M6531N12A2 Demo Board: Bill of Material (Shunt Version)

4.3 71M6531N12A2 DEMO BOARD PCB LAYOUT

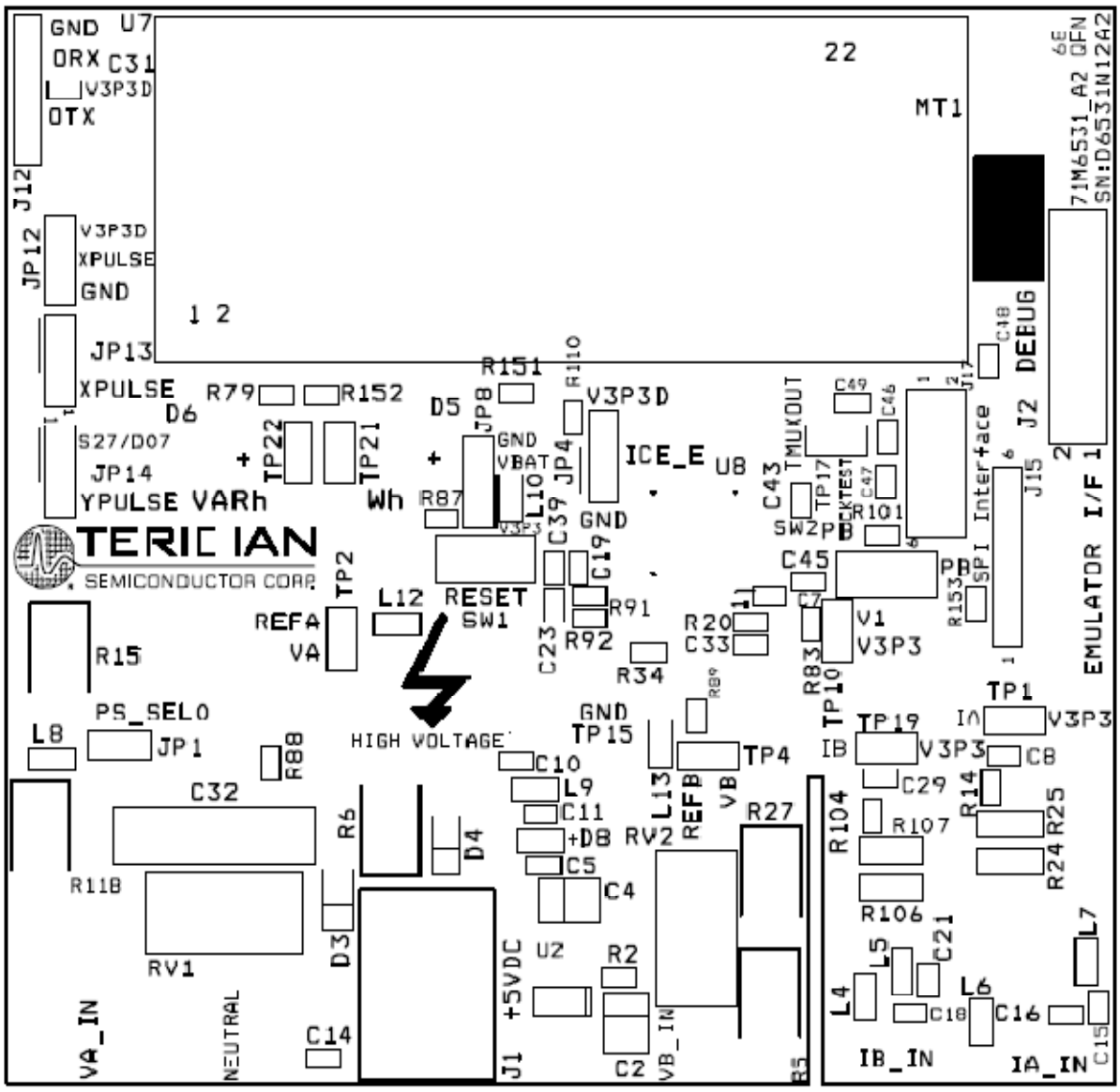

Figure 4-4: 71M6531N12A2 Demo Board: Top Silk Screen

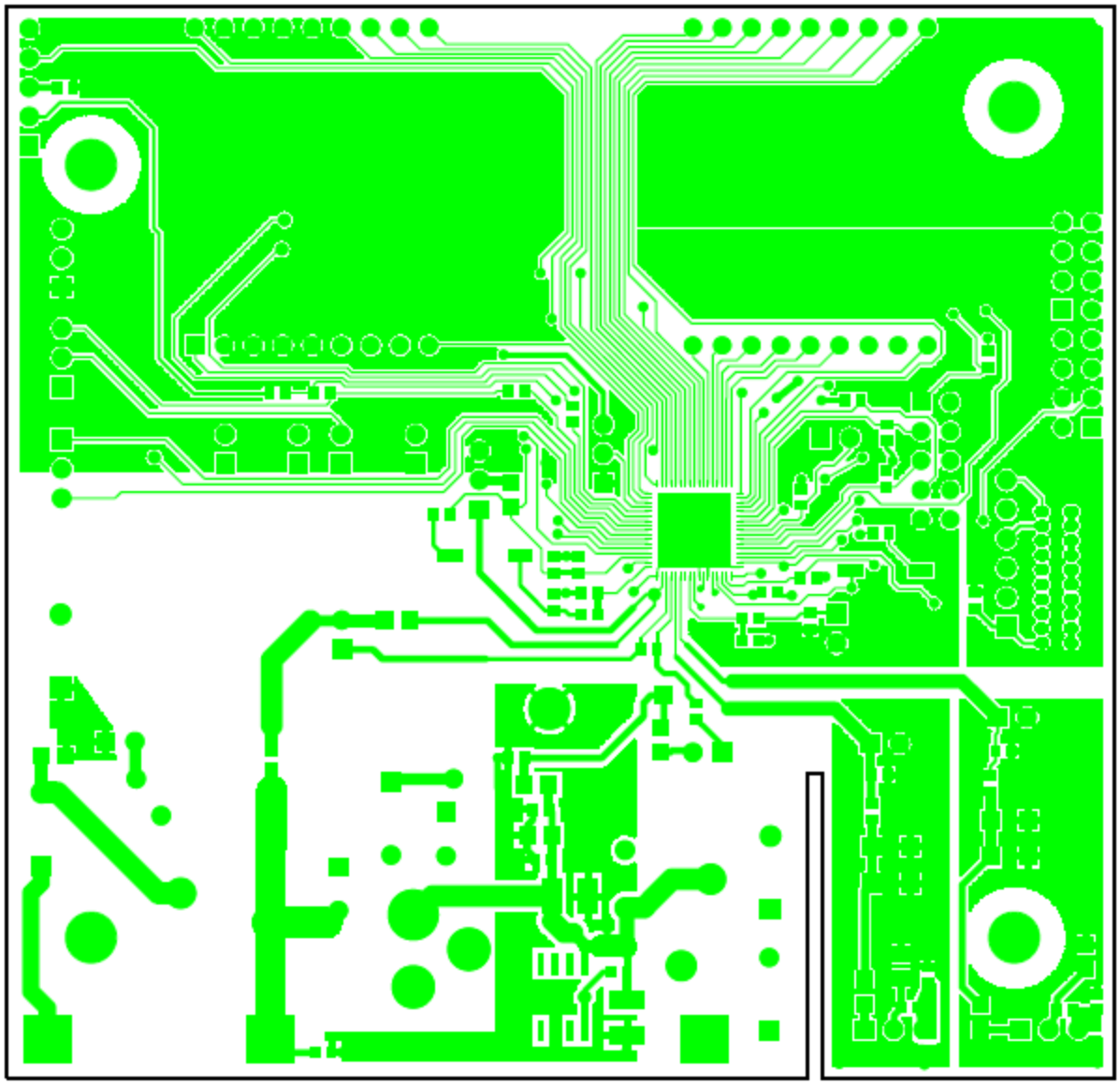

Figure 4-5: 71M6531N12A2 Demo Board: Top Copper Layer

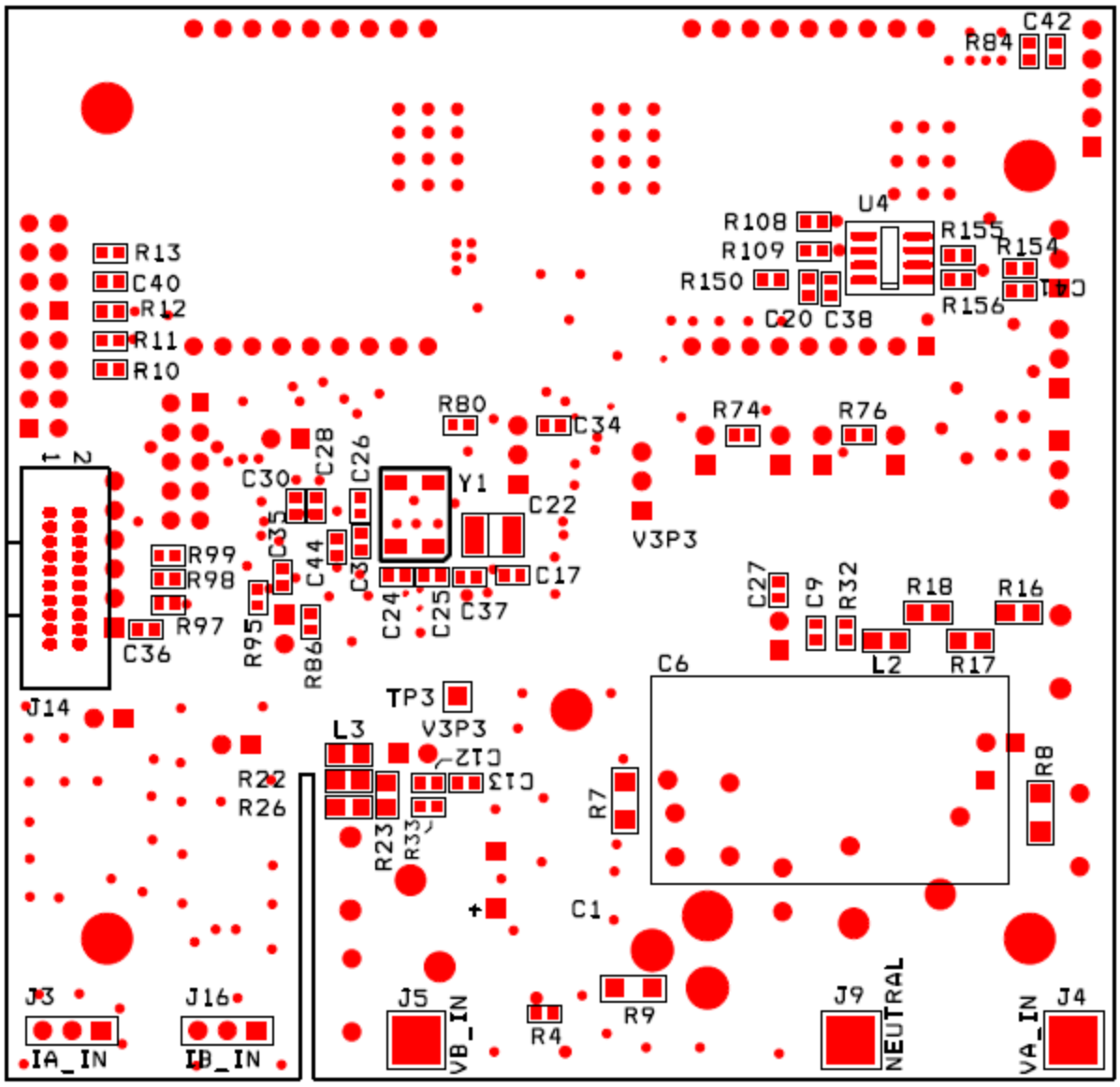

Figure 4-6: 71M6531N12A2 Demo Board: Bottom View with Silk Screen

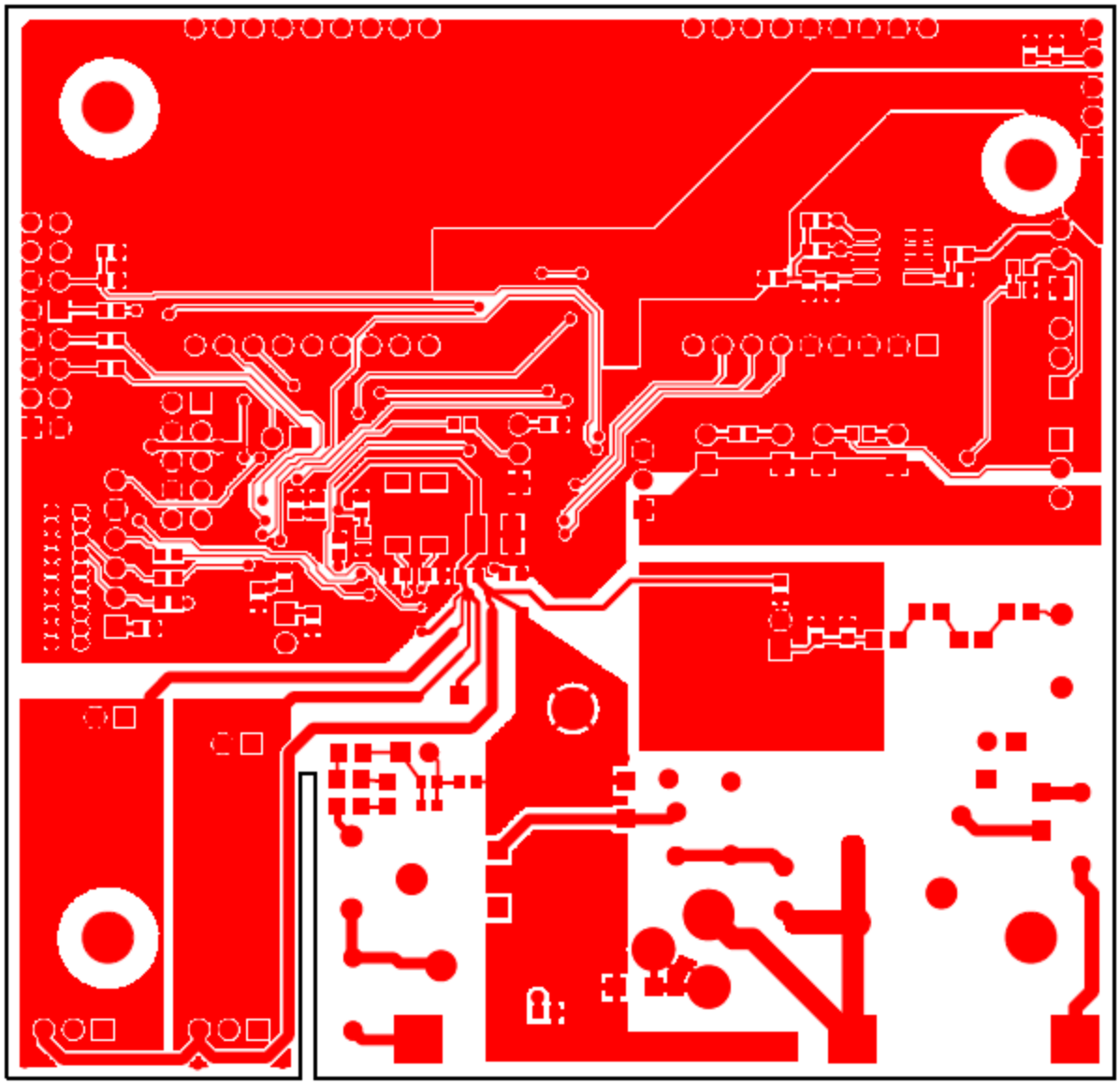

Figure 4-7: 71M6531N12A2 Demo Board: Bottom Copper Layer – Bottom View

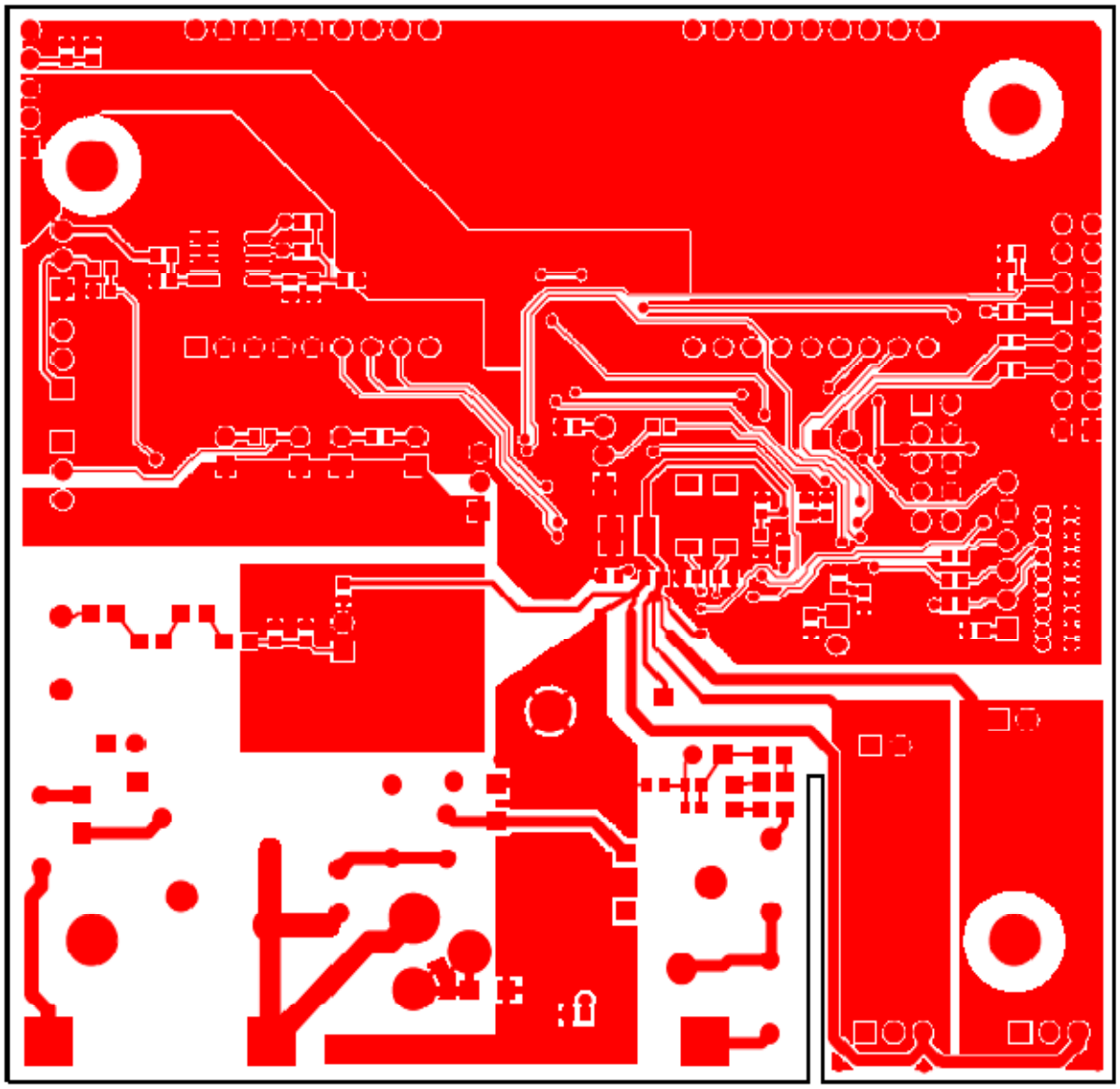

Figure 4-8: 71M6531N12A2 Demo Board: Bottom Copper Layer – Layer View from Top

4.4 DEBUG BOARD BILL OF MATERIAL

Item	Quantity	Reference	Part	PCB Footprint	Digi-Key Part Number	Part Number	Manufacturer
1	21	C1-C3,C5-C10,C12-C23	0.1uF	RC0805	445-1349-1-ND	C2012X7R1H104K	TDK
2	1	C4	33uF, 10V	RC1812	478-1687-1-ND	TAJB336K010R	AVX
3	1	C11	10uF, 16V	RC1812	478-1673-1-ND	TAJB106K016R	AVX
4	2	D2,D3	LED	RC0805	160-1414-1-ND	LTST-C170KGKT	LITEON
5	4	G1,G2,G3,G4	Spacer	MTHOLE	2202K-ND	2202K-ND	Keystone Electronics
6	4		4-40, 1/4" screw		H342-ND	PMS 4400 - 0025 PH	Building Fasteners
7	1	J1	DC Connector	RAPC712X	SC237-ND	RAPC712X	Switchcraft
8	1	J2	DB9, right angle, female	DSUB9_SKT	A32117-ND	5747844-4	AMP/Tyco
9	1	J3	HEADER (F) 8X2	8X2PIN	S7111-ND	PPPC082LFBN-RC	Sullins
10	4	JP1,JP2,JP3,JP4	HEADER 2	2X1PIN	S1011E-36-ND	PZC36SAAN	Sullins
11	4	R1,R5,R7,R8	10K	RC0805	P10KACT-ND	ERJ-6GEYJ103V	Panasonic
12	2	R2,R3	1K	RC0805	P1.0KACT-ND	ERJ-6GEYJ102V	Panasonic
13	1	R4	NC	RC0805	N/A	N/A	N/A
14	1	R6	0	RC0805	P0.0ACT-ND	ERJ-6GEY0R00V	Panasonic
15	1	SW2	PB switch		P8051SCT-ND	EVQ-PJX05M	Panasonic
16	5	U1,U2,U3,U5,U6	ISOLATOR	SOIC8	ADUM1100ARZ-ND	ADUM1100ARZ	ADI
17	2	TP5,TP6	Test Point	--	5011K-ND	5011	Keystone Electronics
18	1	U4	RS232 DRIVER	28SSOP	MAX3237CAI+-ND	MAX3237CAI+	MAXIM

Table 4-2: Debug Board: Bill of Material

4.5 DEBUG BOARD SCHEMATICS

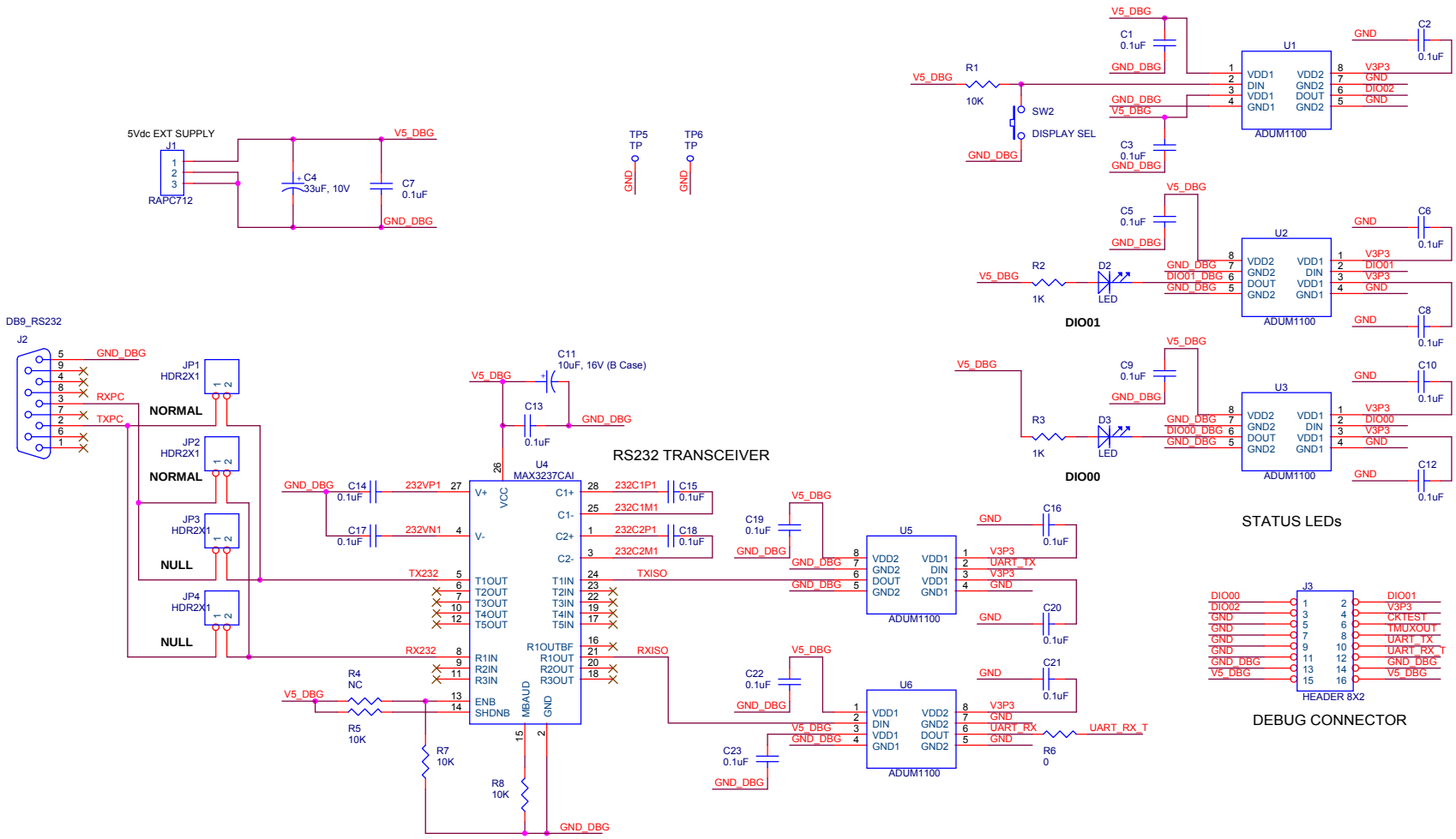

Figure 4-9: Debug Board: Electrical Schematic

4.6 DEBUG BOARD PCB LAYOUT

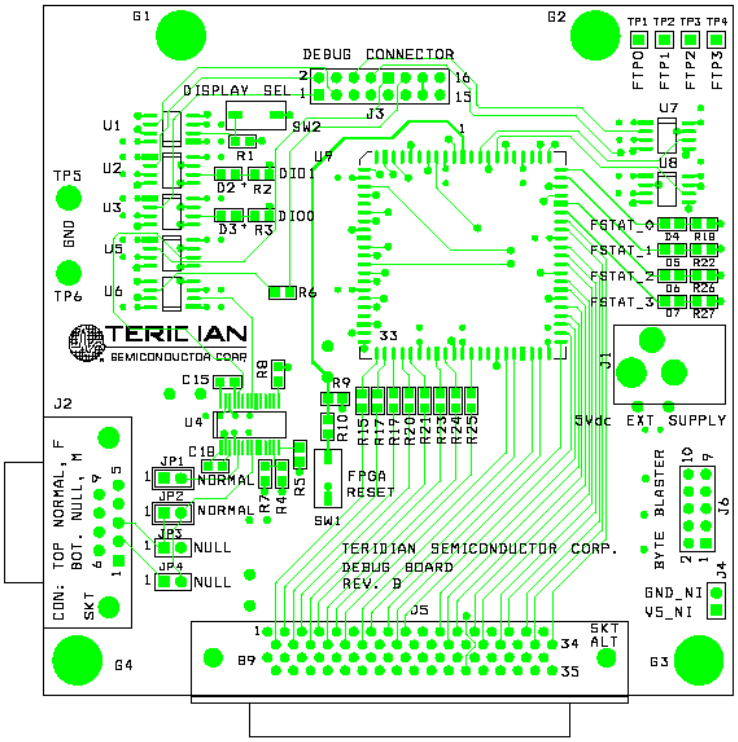

Figure 4-10: Debug Board: Top View

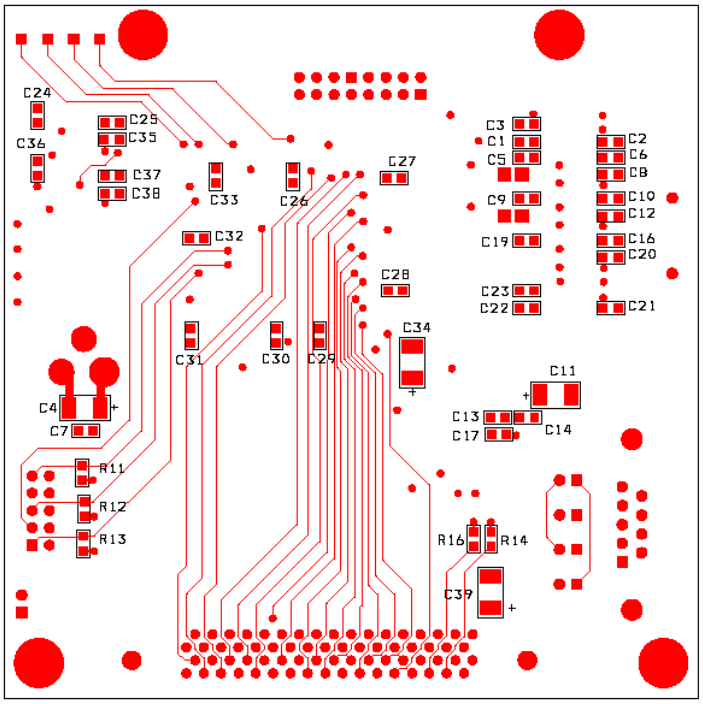

Figure 4-11: Debug Board: Bottom View

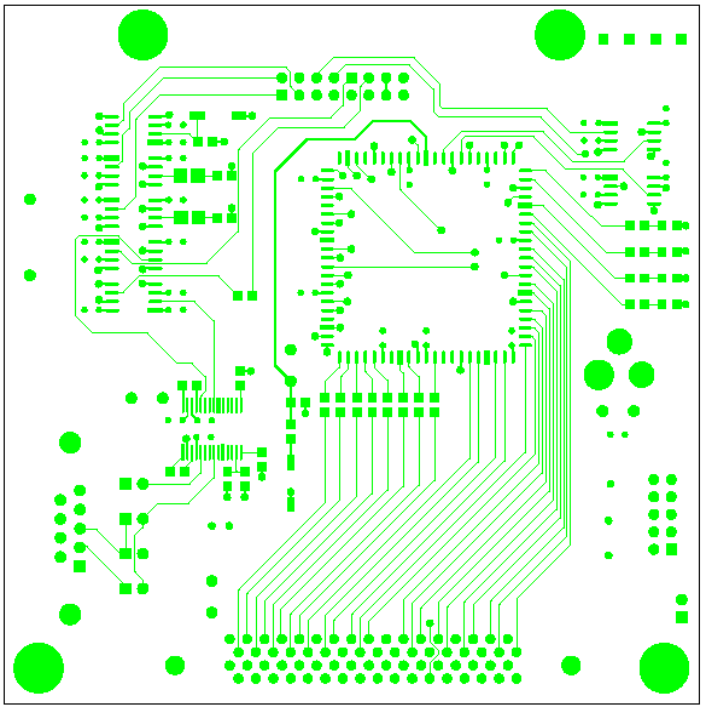

Figure 4-12: Debug Board: Top Signal Layer

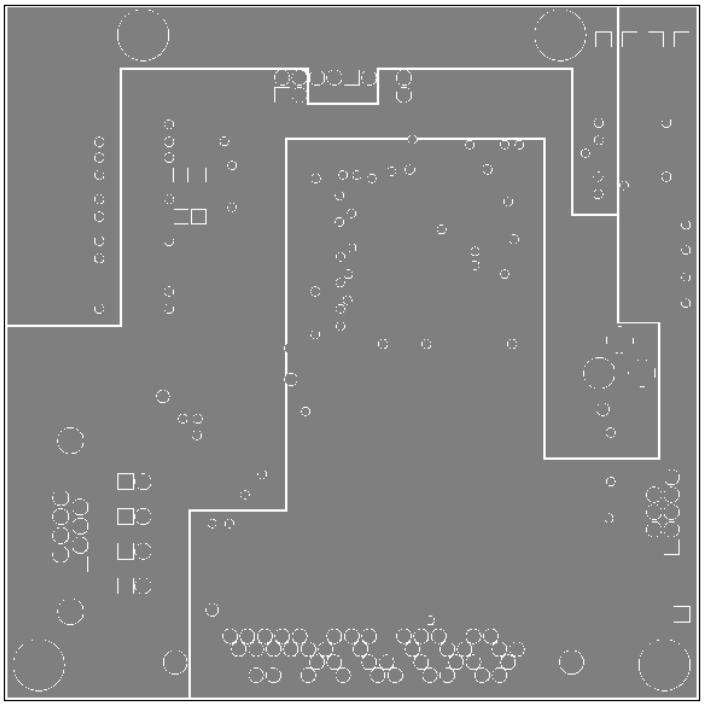

Figure 4-13: Debug Board: Middle Layer 1, Ground Plane

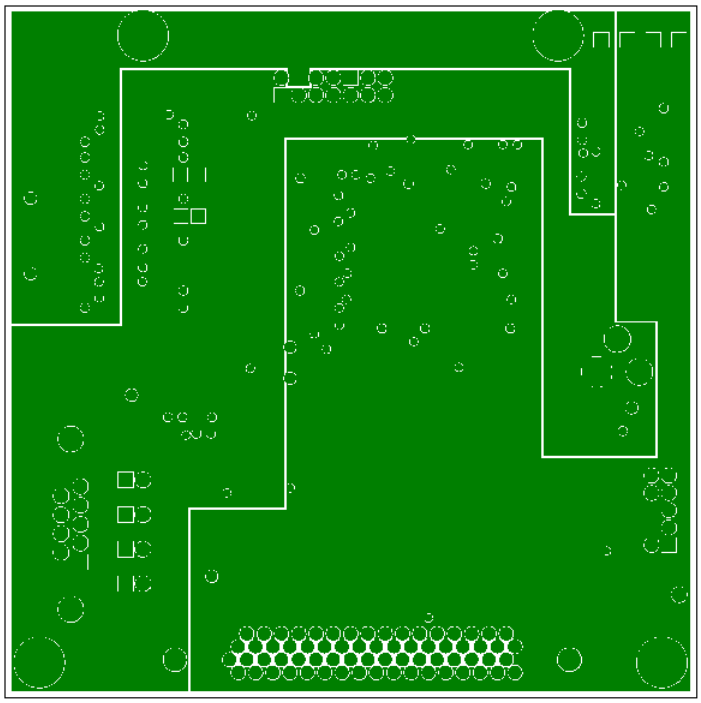

Figure 4-14: Debug Board: Middle Layer 2, Supply Plane

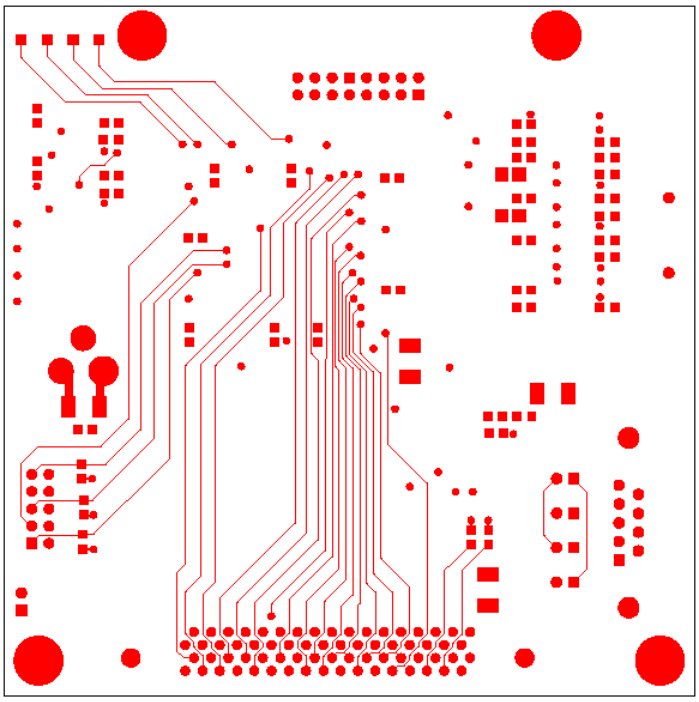

Figure 4-15: Debug Board: Bottom Trace Layer

4.7 TERIDIAN 71M6531D/F PIN-OUT INFORMATION

***Power/Ground/NC Pins*:**

Name	Type	Circuit	Description
GNDA	P	--	Analog ground: This pin should be connected directly to the ground plane.
GNDD	P	--	Digital ground: This pin should be connected directly to the ground plane.
V3P3A	P	--	Analog power supply: A 3.3V power supply should be connected to this pin, must be the same voltage as V3P3SYS.
V3P3SYS	P	--	System 3.3V supply. This pin should be connected to a 3.3V power supply.
V3P3D	O	13	Auxiliary voltage output of the chip, controlled by the internal 3.3V selection switch. In mission mode, this pin is internally connected to V3P3SYS. In BROWNOUT mode, it is internally connected to VBAT. This pin is floating in LCD and sleep mode. Limit the capacitance to GND of this pin to 0.1µF.
VBAT	P	12	Power supply for Battery backup and oscillator circuit. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3SYS.
V2P5	O	10	Output of the internal 2.5V regulator. A 0.1µF capacitor to GNDA should be connected to this pin.

Analog Pins:

Name	Type	Circuit	Description
IA, IB	I	6	Line Current Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of current sensors. **Unused pins must be tied to V3P3A.**
VA, VB	I	6	Line Voltage Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of resistor dividers. **Unused pins must be tied to V3P3A. If unused, VB can also be tied to VA.**
V1	I	7	Comparator Input: This pin is a voltage input to the internal comparator. The voltage applied to the pin is compared to the internal BIAS voltage (1.6V). If the input voltage is above VBIAS, the comparator output will be high (1). If the comparator output is low, a voltage fault will occur. A series 10kΩ resistor should be connected from V1 to the resistor divider.
VREF	O	9	Voltage Reference for the ADC. This pin should be left unconnected.
XIN XOUT	I	8	Crystal Inputs: A 32kHz crystal should be connected across these pins. Typically, a 33pF capacitor is also connected from XIN to GNDA and a 7pF capacitor is connected from XOUT to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer datasheet for details.

Pin types: P = Power, O = Output, I = Input, I/O = Input/O

Table 4-3: 71M6531D/F Pin description 1/2

Digital Pins:

Name	Type	Circuit	Description
COM3, COM2, COM1, COM0	O	5	LCD Common Outputs: These 4 pins provide the select signals for the LCD display.
SEG0…SEG2, SEG7, SEG8, SEG12…SEG18	O	5	Dedicated LCD Segment Output pins.
COM3, COM2, COM1, COM0	O	5	LCD Common Outputs: These 4 pins provide the select signals for the LCD display.
SEG0…SEG2, SEG7, SEG8, SEG12…SEG18	O	5	Dedicated LCD Segment Output pins.
SEG24/DIO4… SEG35/DIO15	I/O	3, 4, 5	Multi-use pins, configurable as either LCD SEG driver or DIO. (DIO4 = SCK, DIO5 = SDA when configured as EEPROM interface, WPULSE = DIO6, VARPULSE = DIO7 when configured as pulse outputs). **Unused pins must be configured as outputs or terminated to V3P3/GNDD.**
SEG37/DIO17 SEG48/DIO28, SEG49/DIO29 SEG63/DIO43… SEG66/DIO46	I/O	3, 4, 5	Multi-use pins, configurable as either LCD SEG driver or DIO. **Unused pins must be configured as outputs or terminated to V3P3/GNDD.**
SEG3/PCLK SEG4/PSDO SEG5/PCSZ SEG6/PSDI	I/O	3, 4, 5	Multi-use pins, configurable as either LCD SEG driver or SPI PORT.
E_RXTX/SEG9	I/O	1, 4, 5	Multi-use pins, configurable as either emulator port pins (when ICE_E pulled high) or LCD SEG drivers (when ICE_E tied to GND).
E_RST/SEG11	I/O	1, 4, 5	
E_TCLK/SEG10	O	4, 5	
ICE_E	I	2	ICE enable. When zero, E_RST, E_TCLK, and E_RXTX become SEG32, SEG33, and SEG38 respectively. For production units, this pin should be pulled to GND to disable the emulator port.
CKTEST/SEG19	O	4, 5	Multi-use pin, configurable as either Clock PLL output or LCD segment driver. Can be enabled and disabled by *CKOUT_EN*.
TMUXOUT	O	4	Digital output test multiplexer. Controlled by *DMUX[3:0].*
OPT_RX/DIO1	I/O	3, 4, 7	Multi-use pin, configurable as either Optical Receive Input or general DIO. When configured as OPT_RX, this pin receives a signal from an external photo-detector used in an IR serial interface. **If this pin is unused it must be configured as an output or terminated to V3P3D or GNDD.**
OPT_TX/DIO2	I/O	3, 4	Multi-use pin, configurable as either Optical LED Transmit Output, WPULSE, RPULSE, or general DIO. When configured as OPT_TX, this pin is capable of directly driving an LED for transmitting data in an IR serial interface.
RESET	I	2	Chip reset: This input pin is used to reset the chip into a known state. For normal operation, this pin is pulled low. To reset the chip, this pin should be pulled high. This pin has an internal 30µA (nominal) current source pull-down. No external reset circuitry is necessary.
RX	I	3	UART input. **If this pin is unused it must be configured as an output or terminated to V3P3D or GNDD.**

TX	O	4	UART output.
TEST	I	7	Enables Production Test. **This pin must be grounded in normal operation.**
PB	I	3	Push button input. This pin must be at GNDD when not active. A rising edge sets the *IE_PB* flag. It also causes the part to wake up if it is in SLEEP or LCD mode. PB does not have an internal pull-up or pull-down.

Table 4-4: 71M6531D/F Pin description 2/2

PINOUT (QFN 68)

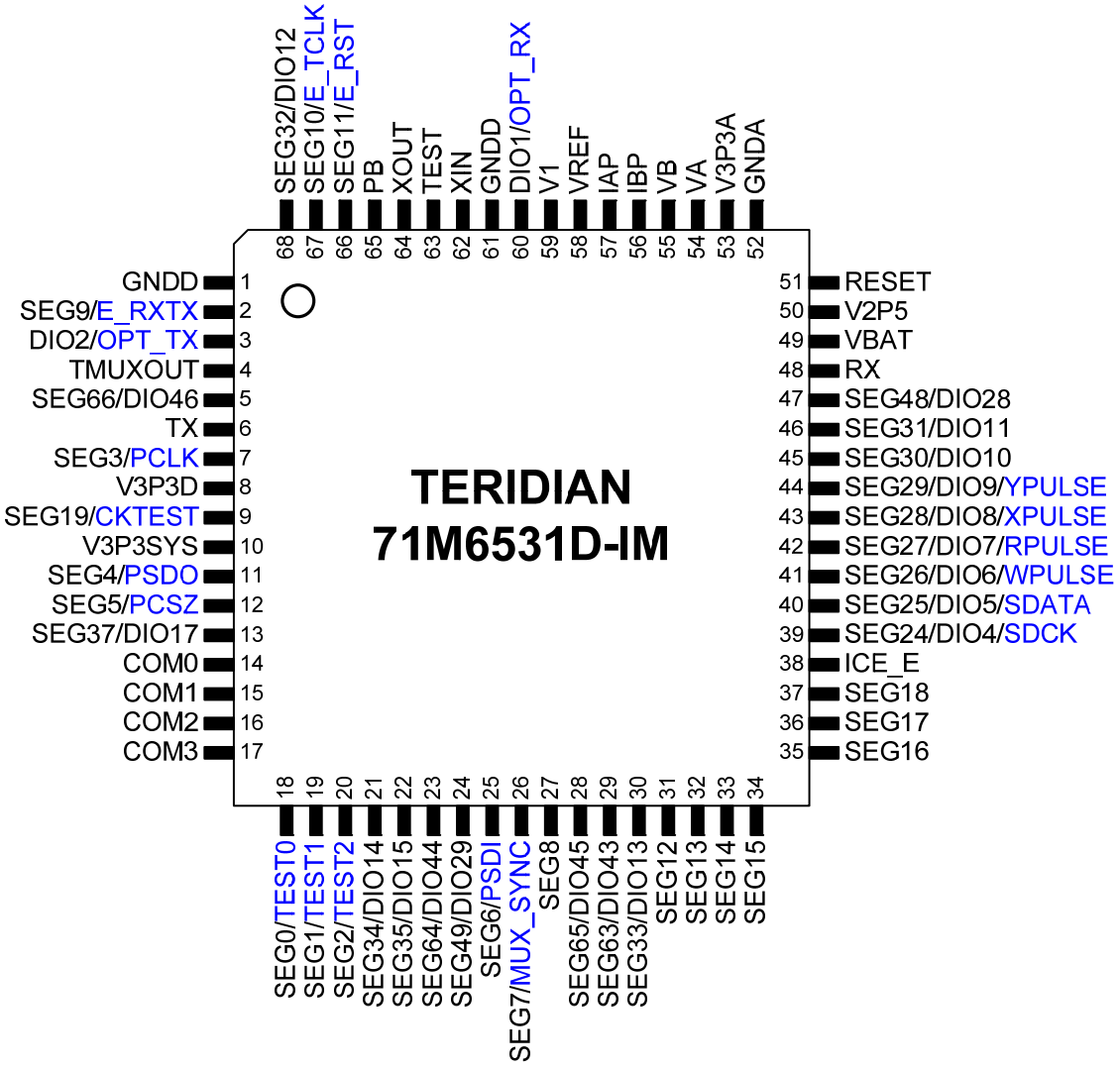

Figure 4-16: TERIDIAN 71M6531D/F LQFP64: Pinout (top view)

4.8 REVISION HISTORY

Revision	Date	Description
1.0	04-13-2007	Initial release
1.1	08-28-2007	Updated referenced to LCD and LCD display options. Updated Tables 1-12 through 1-14.
1.2	10-30-2007	Added description of macro files for adaptation of Demo Code to shunt/CT configurations. Updated list of MPU addresses. Added chapter for RTC Calibration and compensation.
1.3	12-18-2007	Updated schematics, BOM and PCB layout images to Demo Board revision 2.0.
1.4	01-28-2008	Added description of new YPULSE functionality and list of CE locations for Demo Code revision 4p6. Corrected description of]U command, added description of CLS command. Updated kit contents (shunt resistor for shunt configuration only). Added safety notes for emulator operation in section 1.9.5 and to section 1.11.
1.5	06-02-2008	Updated references to latest Demo Code revision. Deleted application circuit diagrams (shown in data sheet) and CE address tables. Updated pin-out diagram (top-view).

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