ANALOG DEVICES

ADP5091-2-EVALZ User Guide
UG-927

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluation Board for the ADP5091 Demonstration Platform for Energy Harvesting

FEATURES

Plug and play energy harvesting platform
Compatible with Analog Devices, Inc., wireless sensor network (WSN) platform
Solar panel harvester included
One regulated output with programmable output voltage
RoHS compliant

GENERAL DESCRIPTION

The ADP5091 demonstration platform is a plug and play evaluation board (ADP5091-2-EVALZ) for energy harvesting. The evaluation board includes the photovoltaic (PV) panel and all of the power management to enable devices to be powered using energy harvesting. It is based on the Alta Device PV cell and the ADP5091 energy harvesting power management IC.

The demonstration platform converts light energy to electrical energy. The PV panel converts the light to 0.8 V electrical energy. The ADP5091 boosts the input voltage from 0.8 V to 3.5 V and stores the energy in a supercapacitor.

The ADP5091 has a regulated output with programmable output voltage. By combining a low dropout (LDO) regulator and a boost regulator, it offers a more compatible output voltage than the output of a main boost regulator. The Alta Device PV cell is a light harvesting, dye sensitized PV cell. It is optimized for indoor environments, where lux levels of 200 lux to 1000 lux are typical.

The ADP5091 is an ultralow power, synchronous, boost dc-to-dc regulator. The ADP5091 runs from input voltages of 0.38 V to 3.3 V and provides a high efficiency solution with integrated power switch, synchronous rectifier, battery management, and one regulated output. The demonstration platform provides an easy way to evaluate the device.

Full details about the ADP5091 are available in the product data sheet, which should be consulted in conjunction with this user guide when using the ADP5091-2-EVALZ.

The system also plugs directly into the Analog Devices WSN demonstration platform.

This user guide describes how to set up the board and how to use it for powering loads.

SYSTEM BLOCK DIAGRAM

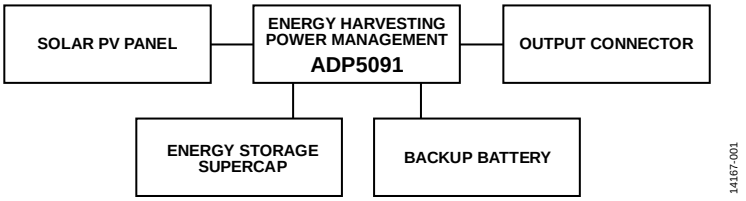

Figure 1.

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REVISION HISTORY

5/2016—Revision 0: Initial Version

EVALUATION BOARD QUICK START GUIDE

This section explains how to connect the solar panel to the evaluation board and how to configure the evaluation board to start up and run.

1. Connect the 10-pin connector on the solar panel to the J3 10-pin connector on the evaluation board, as shown in Figure 2.

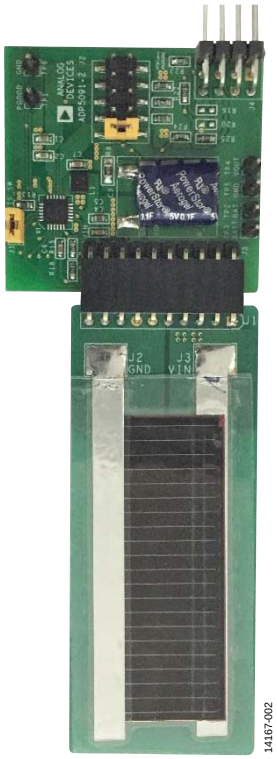

Figure 2. ADP5090-2-EVALZ Hardware

2. Connect J2_1 and J2_2 on the evaluation board, as shown in Figure 3.
3. Place the system in a bright environment. Monitor the voltage on the supercapacitor using the TP3 (BATT) and TP5 (GND) test points.
4. The output is available on J4_1 on the evaluation board.

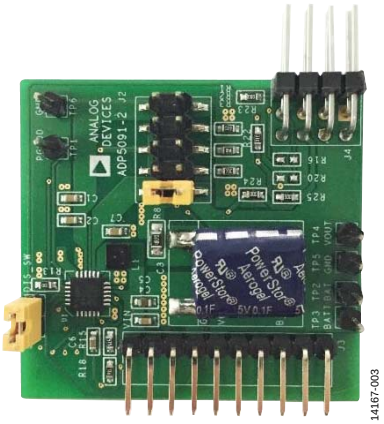

Figure 3. Jumper Setup

EVALUATION BOARD HARDWARE

POWER MANAGEMENT OF THE OUTPUT (LDO)

The ADP5091 has an additional regulated output containing an LDO and a boost. On this evaluation board, the boost is always shut down. With the options of different resistor values, the LDO can generate different output voltages. Table 1 shows the jumper connections and the corresponding output voltage on the ADP5091-2-EVALZ. See the Evaluation Board Schematic section for more details.

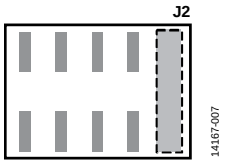

Figure 4. Jumper Position on Evaluation Board for Setting 1

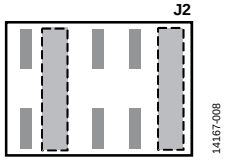

Figure 5. Jumper Position on Evaluation Board for Setting 2

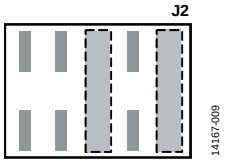

Figure 6. Jumper Position on Evaluation Board for Setting 3

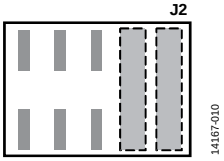

Figure 7. Jumper Position on Evaluation Board for Setting 4

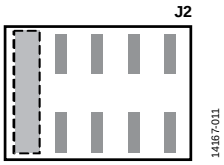

Figure 8. Jumper Position on Evaluation Board for Setting 5

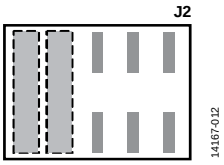

Figure 9. Jumper Position on Evaluation Board for Setting 6

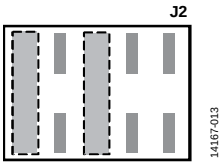

Figure 10. Jumper Position on Evaluation Board for Setting 7

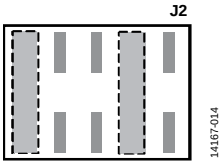

Figure 11. Jumper Position on Evaluation Board for Setting 8

Table 1. Power Management of Sensor Nodes[1]

Setting	V_{OUT} (V)	REG_OUT (V)	Jumper Position
1	V_{SYS}[2]	2.5 V	J2_9 connected to J2_10 (see Figure 4)
2	V_{SYS}[2]	3.3 V	J2_3 connected to J2_4, J2_9 connected to J2_10 (see Figure 5)
3	V_{SYS}[2]	3 V	J2_5 connected to J2_6, J2_9 connected to J2_10 (see Figure 6)
4	V_{SYS}[2]	2.8 V	J2_7 connected to J2_8, J2_9 connected to J2_10 (see Figure 7)
5	2.5 V	2.5 V	J2_1 connected to J2_2 (see Figure 8)
6	3.3 V	3.3 V	J2_1 connected to J2_2, J2_3 connected to J2_4 (see Figure 9)
7	3 V	3 V	J2_1 connected to J2_2, J2_5 connected to J2_6 (see Figure 10)
8	2.8 V	2.8 V	J2_1 connected to J2_2, J2_7 connected to J2_8 (see Figure 11)

[1] Do not connect both J2_1 to J2_2 and J2_9 to J2_10 at the same time.
[2] V_{SYS} means the voltage on the SYS pin.

J4 OUTPUT CONNECTOR

The J4 output connector (see Figure 12) connects the evaluation board to the load. In addition to providing power, J4 also provides other interface connections that allow more interaction between the evaluation board and the host microcontroller unit (MCU) on the load. The evaluation board is directly compatible with the Analog Devices WSN demonstration boards. Table 2 shows the pinout of the J4 output connector and a brief description of the pin functions.

Table 2. J4 Output Connector

Pin No.	Mnemonic	Description
1	VOUT	Output voltage supply from the evaluation board to the load
2	PGOOD	PGOOD output signal from the ADP5091
3	GND	Ground
4	DIS_SW	DIS_SW input signal to the ADP5091
5	BATT	Supercapacitor voltage (for battery monitoring)
6	EN	Enable LDO
7	BACK_UP	Backup voltage (for battery monitoring)
8	REG_OUT	Regulated output voltage supply from the evaluation board to the load

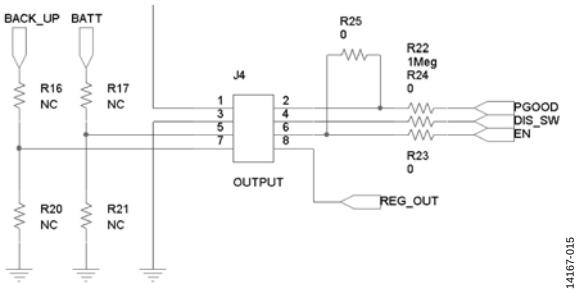

Figure 12. J4 Output Connector

A detailed description of each J4 output connector pin follows:

- The VOUT pin (Pin 1) is the output voltage that the evaluation board delivers to the load.
- The ADP5091 has a programmable PGOOD signal. When the PGOOD threshold is reached, the ADP5091 sets the PGOOD pin (Pin 2) high. It is connected to the host MCU general-purpose input/output (GPIO) input. See the ADP5091 data sheet for more detailed information on this function.
- The GND pin (Pin 3) is the ground connection for the ADP5091.
- Connect the DIS_SW pin (Pin 4) to the host MCU GPIO output. If the host MCU requires the ADP5091 to temporarily halt the switching regulator function, set this pin high. Remove the J1 jumper at the same time, if this function needs to be used. See the ADP5091 data sheet for more detailed information on this function.
- Connect the BATT pin (Pin 5) to the analog input of the host MCU to monitor the voltage on the supercapacitor of the ADP5091-2-EVALZ. Populating R17 and R21 creates a resistor divider for cases where the MCU analog input range is lower than the supercapacitor voltage.
- The EN pin (Pin 6) is the enable control signal for the regulated output. Connect this pin to the host MCU GPIO output to enable or disable the LDO. Also remove R25 if this function needs to be used.
- Connect the BACK_UP pin (Pin 7) to the analog input of the host MCU to monitor the voltage on the backup battery of the ADP5091-2-EVALZ. Populating R16 and R20 creates a resistor divider for cases where the MCU analog input range is lower than the supercapacitor voltage.
- The REG_OUT pin provides an additional output with a different voltage than VOUT when VOUT is using bypass mode (see Table 1).

EVALUATION BOARD SCHEMATICS

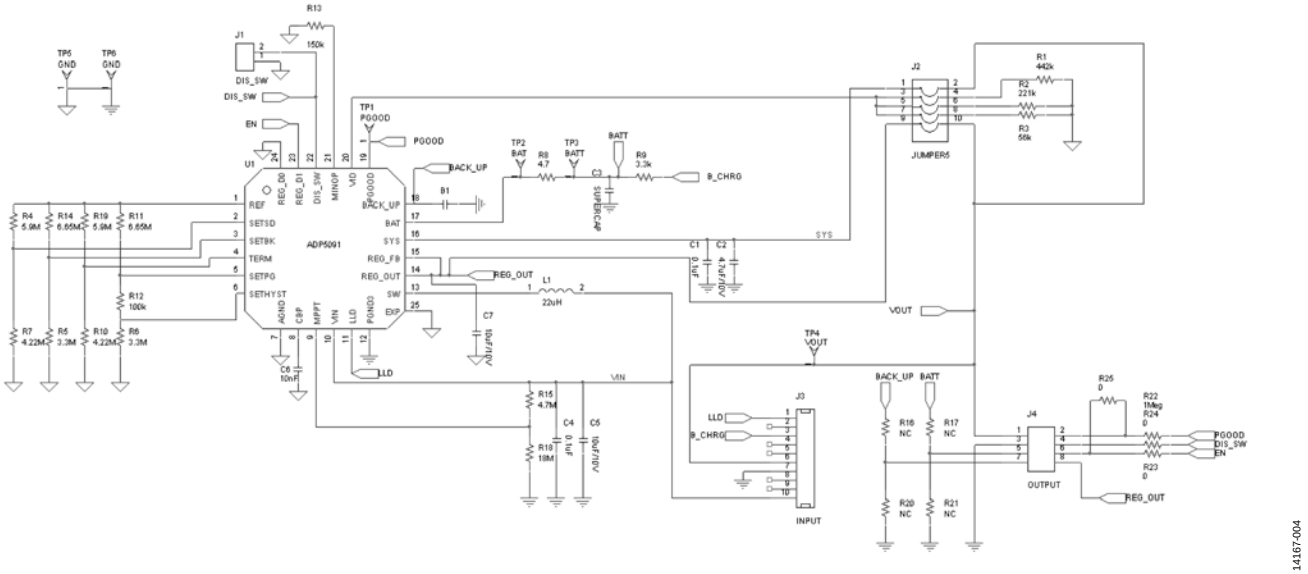

Figure 13. ADP5091-2-EVALZ Evaluation Board Schematic

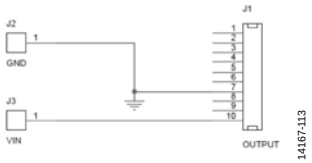

Figure 14. ADP5091-2-EVALZ PV Board Schematic

EVALUATION BOARD LAYOUT

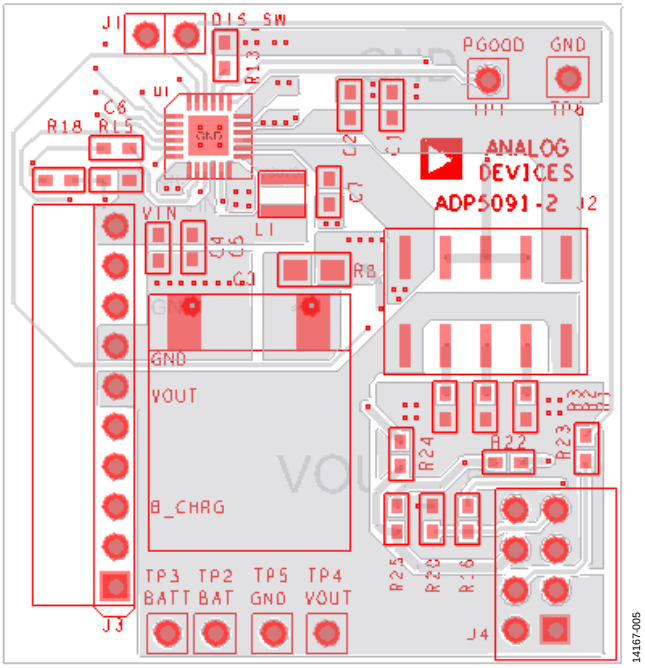

Figure 15. Top Assembly

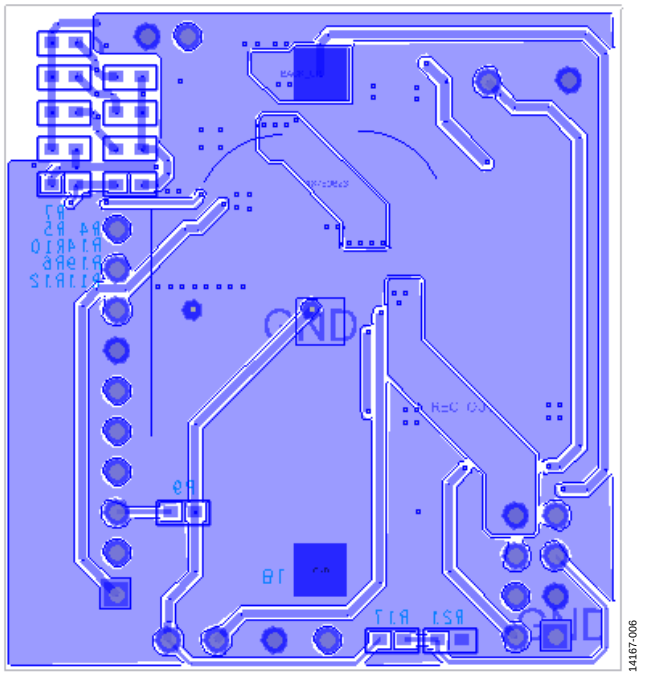

Figure 16. Bottom Assembly

ORDERING INFORMATION

BILL OF MATERIALS

Table 3. Bill of Materials of Evaluation Board

Qty	Reference Designator	Description	Part Number	Vendor
1	B1	CR2032 holder	BC2032-F1	Memory Protection Devices
2	C1, C4	0.1 µF capacitors, C0603	GRM188R71H104KA93	Murata
2	C2, C5	4.7 µF, 10 V capacitors, C0603	GRM21BR61A475KA73	Murata
1	C3	Supercapacitor, 12 × 12	PB-5R0H104-R	Cooper Bussmann
1	C6	10 nF capacitor, C0603	GRM188R71H103KA01	Murata
1	C7	10 µF, 10 V capacitors, C0603	GRM188R61A106KE69D	Murata
1	J1	DIS_SW jumper, SIP2	61304011121	Würth Elektronik
1	J2	V_{OUT} and REG_OUT setting jumper, SIP10_dual	61031021121	Würth Elektronik
1	J3	Input jumper, SIP10_BtoB	61301011021	Würth Elektronik
1	J4	Output jumper, SIP8_2rows	9-103324-0	TE Connectivity
1	L1	22 µH inductor, 3 × 3	EPL3015-223ML, 744025220	Coilcraft, Würth Elektronik
1	R1	442 kΩ resistor, R0603	CRCW0603442KFKEA	Vishay Dale
1	R2	221 kΩ resistor, R0603	CRCW0603221KFKEA	Vishay Dale
1	R3	56 kΩ resistor, R0603	CRCW060356K0FKEA	Vishay Dale
2	R4, R19	5.9 MΩ resistor, R0603	CRCW06035M90FKEA	Vishay Dale
2	R5, R6	3.3 MΩ resistor, R0603	CRCW06033M30FKEA	Vishay Dale
2	R7, R10	4.22 MΩ resistors, R0603	CRCW06034M22FKEA	Vishay Dale
1	R8	4.7 Ω resistor, R0805	CRCW08054R70JNEAIF	Vishay Dale
1	R9	3.3 kΩ resistor, R0603	CRCW06033K30FKEA	Vishay Dale
2	R11, R14	6.65 MΩ resistor, R0603	CRCW06036M65FKEA	Vishay Dale
1	R12	100 kΩ resistor, R0603	CRCW0603100KFKEA	Vishay Dale
1	R13	150 kΩ resistor, R0603	CRCW0603150KFKEA	Vishay Dale
1	R15	4.7 MΩ resistor, R0603	CRCW06034M70FKEA	Vishay Dale
4	R16, R17, R20, R21	No connect (NC) resistors, R0603	Not applicable	Not applicable
1	R18	18 MΩ resistor, R0603	CRCW060318M0JPEAHR	Vishay Dale
1	R22	1 MΩ resistor, R0603	CRCW06031M00FKEA	Vishay Dale
3	R23, R24, R25	0 Ω resistor, R0603	CRCW06030000Z0EA	Vishay Dale
1	TP1	PGOOD test point, SIP1	61304011121	Würth Elektronik
1	TP2	BAT test point, SIP1	61304011121	Würth Elektronik
1	TP3	BATT test point, SIP1	61304011121	Würth Elektronik
1	TP4	VOUT test points, SIP1	61304011121	Würth Elektronik
2	TP5, TP6	GND test points, SIP1	61304011121	Würth Elektronik
1	U1	ADP5091 24-lead LFCSP	ADP5091ACPZ-1-R7	Analog Devices

Table 4. Bill of Materials of PV Board

Qty	Reference Designator	Description	Part Number	Vendor
1	J1	Output jumper, SIP10	613010143121	Würth Elektronik
1	J2	Input 1 jumper, PV_INPUT	Not applicable	Alta Device
1	J3	Input 2 jumper, PV_INPUT	Not Applicable	Alta Device

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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